SONY

Diagonal 8.86 mm (Type 1/1.8) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

IMX334LQR-C

STARVIS

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Description

The IMX334LQR-C is a diagonal 8.86 mm (Type 1/1.8) CMOS active pixel type solid-state image sensor with a square pixel array and 8.42 M effective pixels. This chip operates with analog 2.9 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- ◆CMOS active pixel type dots
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Input frequency: 6 to 27 MHz / 37.125 MHz / 74.25 MHz
- ◆Number of recommended recording pixels: 3840 (H) × 2160 (V) approx. 8.29M pixel
- ◆Readout mode
  - All-pixel scan mode
  - Horizontal/Vertical 2/2-line binning mode
  - Window cropping mode
  - Vertical / Horizontal direction-normal / inverted readout mode
- ◆Readout rate
  - Maximum frame rate in All-pixel scan mode 3840(H)×2160(V) AD12bit: 60 frame / s
- ◆High dynamic range (HDR) function
  - Multiple exposure HDR
  - Digital overlap HDR
- ◆Variable-speed shutter function (resolution 1H units)
- ◆10-bit / 12-bit A/D converter
- ◆CDS / PGA function
  - 0 dB to 30dB : Analog Gain 30dB (step pitch 0.3 dB)
  - 30.3 dB to 72dB : Analog Gain 30dB + Digital Gain 0.3 to 42dB (step pitch 0.3 dB)
- ◆Supports I/O
  - CSI-2 serial data output (4 Lane / 8 Lane, RAW10 / RAW12 output)
- ◆Recommended exit pupil distance: –30 mm to –∞

E17Y08A84

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Type 1/1.8
- ◆ Total number of pixels
  3952 (H) × 2320 (V) approx. 9.17 M pixels
- ◆ Number of effective pixels
  3864 (H) × 2180 (V) approx. 8.42 M pixels
- ◆ Number of active pixels
  3864 (H) × 2176 (V) approx. 8.41 M pixels
- ◆ Number of recommended recording pixels
  3840 (H) × 2160 (V) approx. 8.29 M pixels
- ◆ Unit cell size
  2.0 µm (H) × 2.0 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 13 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 0 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 1 : 2.9 V)	AV_{DD1}	-0.3	3.3	V	
Supply voltage (analog 2 : 2.9 V)	AV_{DD2}	-0.3	3.3	V	
Supply voltage (interface 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital1 : 1.2 V)	DV_{DD1}	-0.3	2.0	V	
Supply voltage (digital 2 : 1.2 V)	DV_{DD2}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V

Application Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 1 : 2.9 V)	AV_{DD1}	2.80	2.90	3.00	V
Supply voltage (analog 2 : 2.9 V)	AV_{DD2}	2.80	2.90	3.00	V
Supply voltage (interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital1 : 1.2 V)	DV_{DD1}	1.10	1.20	1.30	V
Supply voltage (digital 2 : 1.2 V)	DV_{DD2}	1.10	1.20	1.30	V
Performance guarantee temperature	Tspec	-10	—	60	˚C
Operating guarantee temperature	Topr	-30	—	85	˚C
Storage guarantee temperature	Tstg	-40	—	85	˚C

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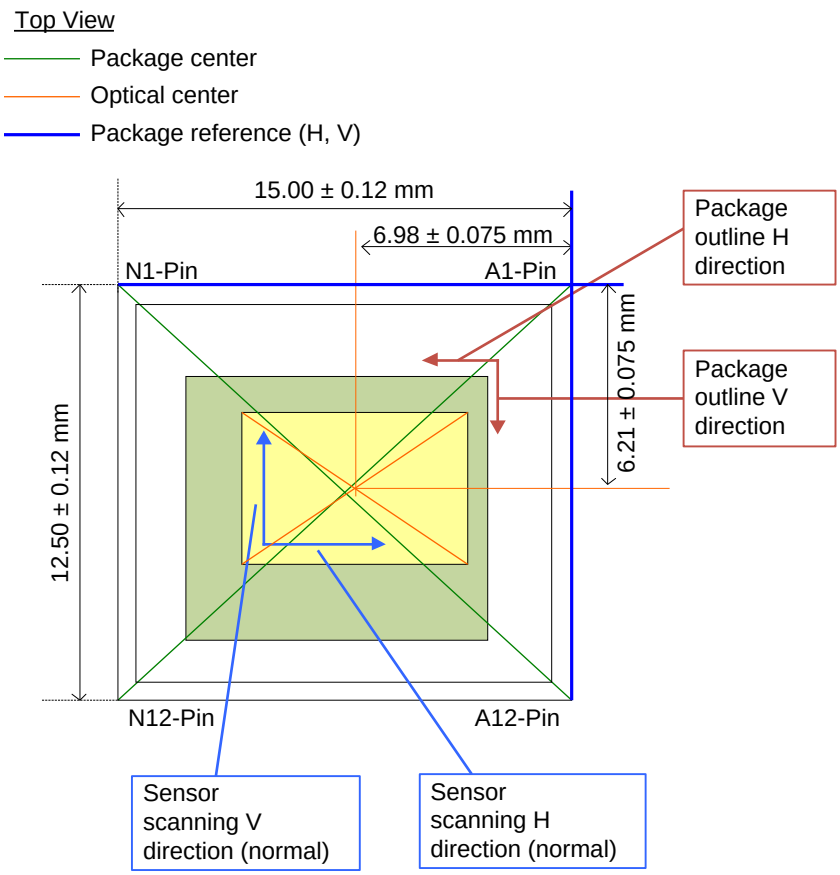
General-0.0.9

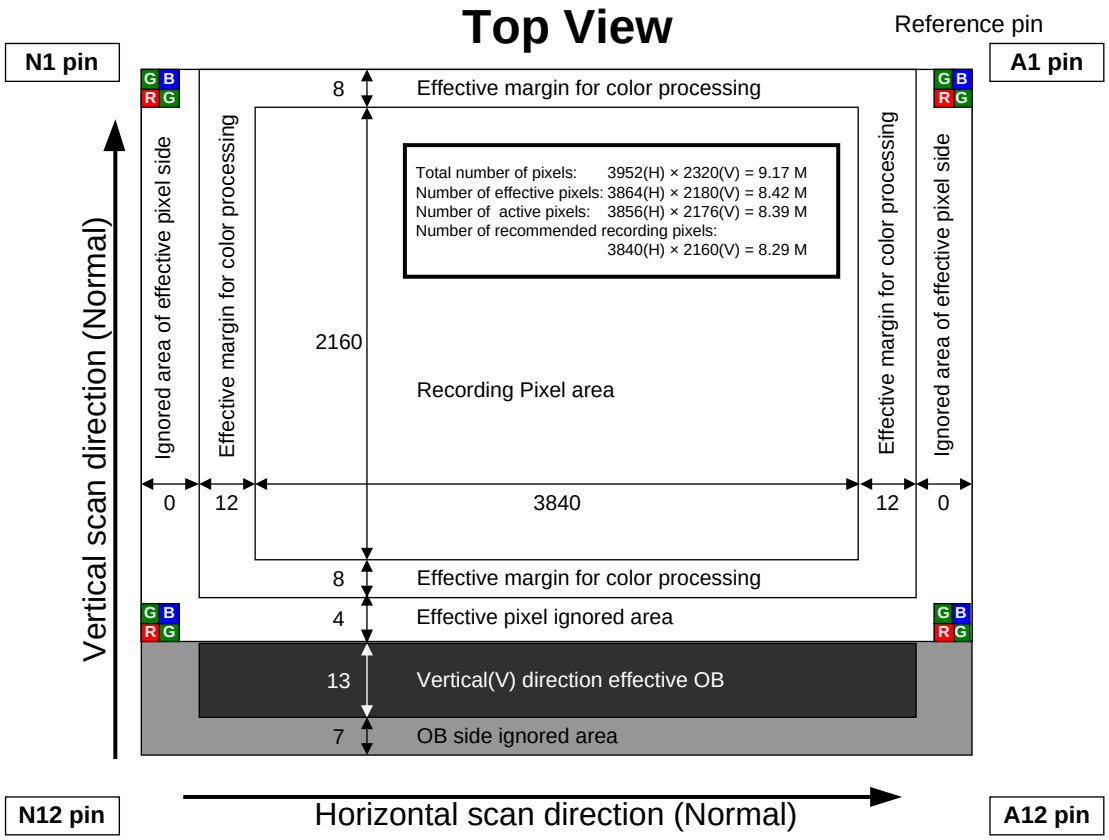
Contents

Optical Center



Optical Center

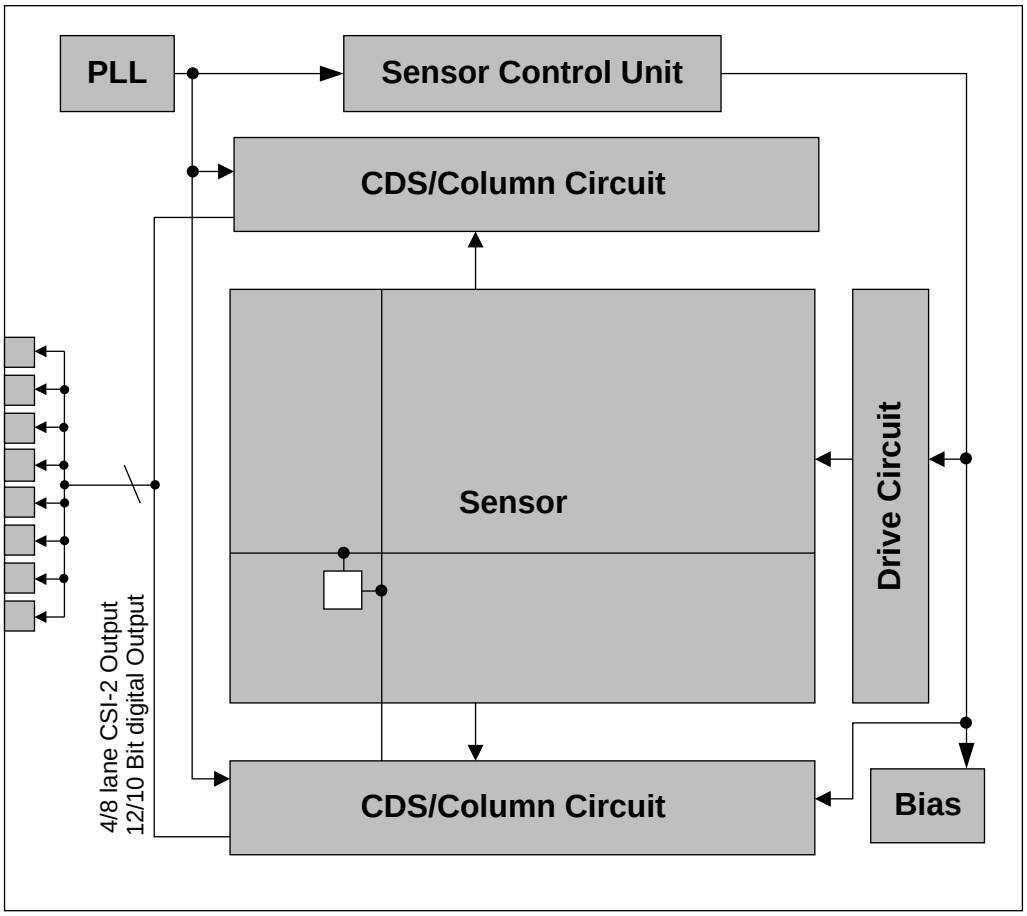
Pixel Arrangement



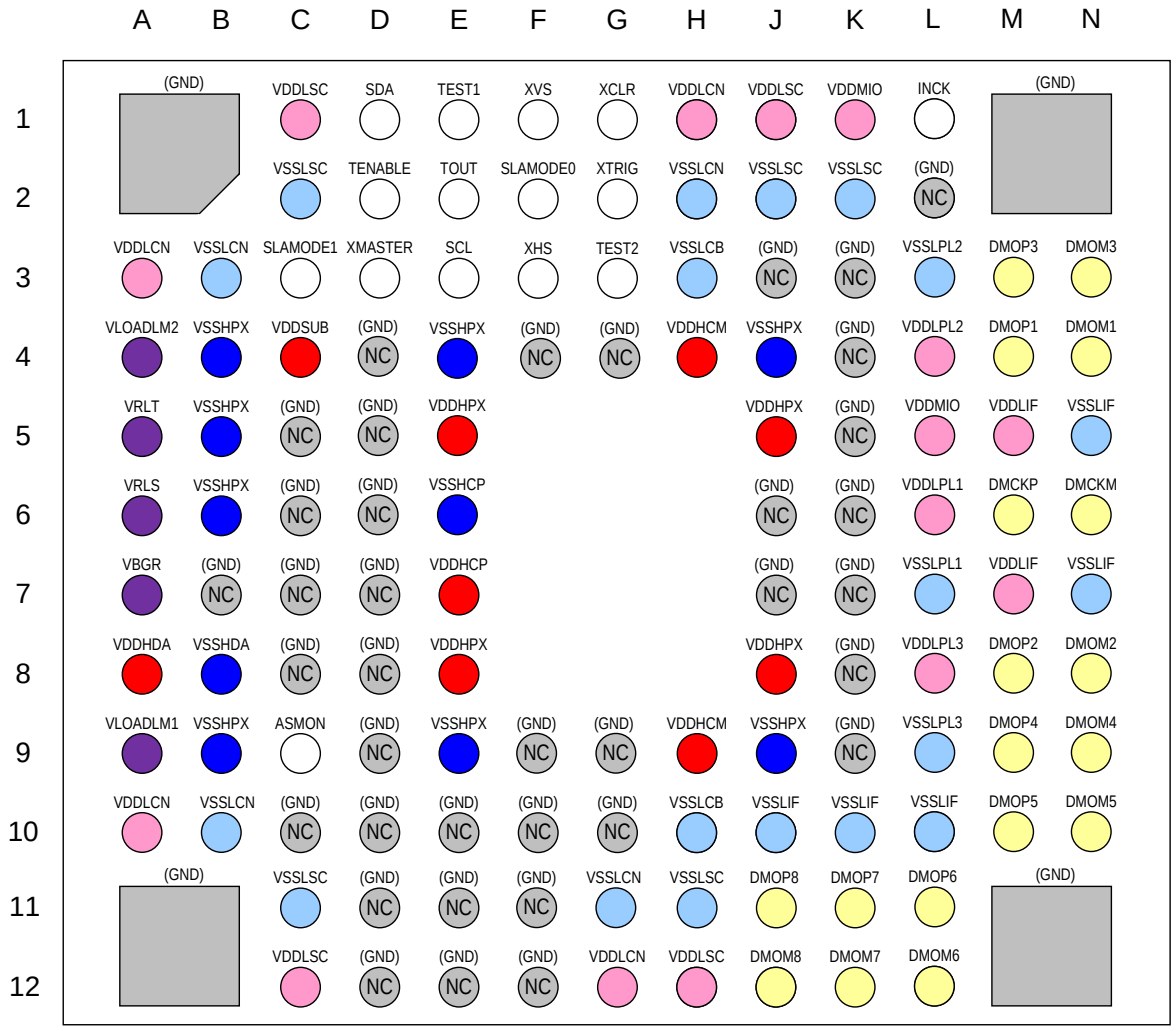
* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.

Pixel Arrangement (Top View)

Block Diagram and Pin Configuration



Block Diagram



*The N.C. pin can be connected to GND.

Pin Configuration (Bottom View)

Pin Description

No.	Pin No	I/O	A/D	Symbol	Description	Remarks
1	A1	—	—	N.C.	—	GND connectable
2	A2	—	—	N.C.	—	GND connectable
3	A3	Power	D	VDDLCN	1.2 V power supply	
4	A4	O	A	VLOADLM2	Capacitor connection	
5	A5	O	A	VRLT	Capacitor connection	
6	A6	O	A	VRLS	Capacitor connection	
7	A7	O	A	VBGR	Capacitor connection	
8	A8	Power	A	VDDHDA	2.9 V power supply	
9	A9	O	A	VLOADLM1	Capacitor connection	
10	A10	Power	D	VDDLCN	1.2 V power supply	
11	A11	—	—	N.C.	—	GND connectable
12	A12	—	—	N.C.	—	GND connectable
13	B1	—	—	N.C.	—	GND connectable
14	B2	—	—	N.C.	—	GND connectable
15	B3	GND	D	VSSLCN	1.2 V GND	
16	B4	GND	A	VSSHPX.	2.9 V GND	
17	B5	GND	A	VSSHPX	2.9 V GND	
18	B6	GND	A	VSSHPX	2.9 V GND	
19	B7	—	—	N.C.	—	GND connectable
20	B8	GND	A	VSSHDA	2.9 V GND	
21	B9	GND	A	VSSHPX	2.9 V GND	
22	B10	GND	D	VSSLCN	1.2 V GND	
23	B11	—	—	N.C.	—	GND connectable
24	B12	—	—	N.C.	—	GND connectable
25	C1	Power	D	VDDLSC	1.2 V power supply	
26	C2	GND	D	VSSLSC	1.2 V GND	
27	C3	I	D	SLAMODE1	Reference pin	Select slave address
28	C4	Power	A	VDDSUB	2.9 V power supply	
29	C5	—	—	N.C.	—	GND connectable
30	C6	—	—	N.C.	—	GND connectable
31	C7	—	—	N.C.	—	GND connectable
32	C8	—	—	N.C.	—	GND connectable
33	C9	O	A	ASMON	TEST output pin	OPEN
34	C10	—	—	N.C.	—	GND connectable
35	C11	GND	D	VSSLSC	1.2 V GND	
36	C12	Power	D	VDDLSC	1.2 V power supply	
37	D1	I/O	D	SDA	Serial data communication	I^2C: SDA pin
38	D2	I	D	TENABLE	TEST Enable	OPEN
39	D3	I	D	XMASTER	Master / Slave selection	High: Slave mode Low: Master mode
40	D4	—	—	N.C.	—	GND connectable
41	D5	—	—	N.C.	—	GND connectable
42	D6	—	—	N.C.	—	GND connectable
43	D7	—	—	N.C.	—	GND connectable

No.	Pin No	I/O	A/D	Symbol	Description	Remarks
44	D8	—	—	N.C.	—	GND connectable
45	D9	—	—	N.C.	—	GND connectable
46	D10	—	—	N.C.	—	GND connectable
47	D11	—	—	N.C.	—	GND connectable
48	D12	—	—	N.C.	—	GND connectable
49	E1	O	D	TEST1	TEST output pin	OPEN
50	E2	O	D	TOUT	TEST output pin	OPEN
51	E3	I	D	SCL	Serial clock input	I^2C: SCL pin
52	E4	GND	A	VSSHPX	2.9 V GND	
53	E5	Power	A	VDDHPX	2.9 V power supply	
54	E6	GND	A	VSSHCP	2.9 V GND	
55	E7	Power	A	VDDHCP	2.9 V power supply	
56	E8	Power	A	VDDHPX	2.9 V power supply	
57	E9	GND	A	VSSHPX	2.9 V GND	
58	E10	—	—	N.C.	—	GND connectable
59	E11	—	—	N.C.	—	GND connectable
60	E12	—	—	N.C.	—	GND connectable
61	F1	I/O	D	XVS	Vertical sync signal	
62	F2	I	D	SLAMODE0	Reference pin	Select slave address
63	F3	I/O	D	XHS	Horizontal sync signal	
64	F4	—	—	N.C.	—	GND connectable
65	F9	—	—	N.C.	—	GND connectable
66	F10	—	—	N.C.	—	GND connectable
67	F11	—	—	N.C.	—	GND connectable
68	F12	—	—	N.C.	—	GND connectable
69	G1	I	D	XCLR	System clear	High: Normal Low: Clear
70	G2	I	D	XTRIG	Trigger input	
71	G3	I	D	TEST2	TEST pin	Connect to 1.8V power supply
72	G4	—	—	N.C.	—	GND connectable
73	G9	—	—	N.C.	—	GND connectable
74	G10	—	—	N.C.	—	GND connectable
75	G11	GND	D	VSSLCN	1.2 V GND	
76	G12	Power	D	VDDLCN	1.2 V power supply	
77	H1	Power	D	VDDLCN	1.2 V power supply	
78	H2	GND	D	VSSLCN	1.2 V GND	
79	H3	GND	D	VSSLCB	1.2 V GND	
80	H4	Power	A	VDDHCM	2.9 V power supply	
81	H9	Power	A	VDDHCM	2.9 V power supply	
82	H10	GND	D	VSSLCB	1.2 V GND	
83	H11	GND	D	VSSLSC	1.2 V GND	
84	H12	Power	D	VDDLSC	1.2 V power supply	
87	J1	Power	D	VDDLSC	1.2 V power supply	
88	J2	GND	D	VSSLSC	1.2 V GND	
89	J3	—	—	N.C.	—	GND connectable
90	J4	GND	A	VSSHPX	2.9 V GND	
91	J5	Power	A	VDDHPX	2.9 V power supply	
92	J6	—	—	N.C.	—	GND connectable

No.	Pin No	I/O	A/D	Symbol	Description	Remarks
93	J7	—	—	N.C.	—	GND connectable
94	J8	Power	A	VDDHPX	2.9 V power supply	
95	J9	GND	A	VSSHPX	2.9 V GND	
96	J10	GND	D	VSSLIF	1.2 V GND	
97	J11	O	D	DMOP8	CSI-2 output	
98	J12	O	D	DMOM8	CSI-2 output	
99	K1	Power	D	VDDMIO	1.8 V power supply	
100	K2	GND	D	VSSLSC	1.2 V GND	
101	K3	—	—	N.C.	—	GND connectable
102	K4	—	—	N.C.	—	GND connectable
103	K5	—	—	N.C.	—	GND connectable
104	K6	—	—	N.C.	—	GND connectable
105	K7	—	—	N.C.	—	GND connectable
106	K8	—	—	N.C.	—	GND connectable
107	K9	—	—	N.C.	—	GND connectable
108	K10	GND	D	VSSLIF	1.2 V GND	
109	K11	O	D	DMOP7	CSI-2 output	
110	K12	O	D	DMOM7	CSI-2 output	
111	L1	I	D	INCK	Master clock input	
112	L2	—	—	N.C.	—	GND connectable
113	L3	GND	A	VSSLPL2	1.2 V GND	
114	L4	Power	A	VDDLPL2	1.2 V power supply	
115	L5	Power	D	VDDMIO	1.8 V power supply	
116	L6	Power	A	VDDLPL1	1.2 V power supply	
117	L7	GND	A	VSSLPL1	1.2 V GND	
118	L8	Power	A	VDDLPL3	1.2 V power supply	
119	L9	GND	A	VSSLPL3	1.2 V GND	
120	L10	GND	D	VSSLIF	1.2 V GND	
121	L11	O	D	DMOP6	CSI-2 output	
122	L12	O	D	DMOM6	CSI-2 output	
123	M1	—	—	N.C.	—	GND connectable
124	M2	—	—	N.C.	—	GND connectable
125	M3	O	D	DMOP3	CSI-2 output	
126	M4	O	D	DMOP1	CSI-2 output	
127	M5	Power	D	VDDLIF	1.2 V power supply	
128	M6	O	D	DMCKP	CSI-2 output	
129	M7	Power	D	VDDLIF	1.2 V power supply	
130	M8	O	D	DMOP2	CSI-2 output	
131	M9	O	D	DMOP4	CSI-2 output	
132	M10	O	D	DMOP5	CSI-2 output	
133	M11	—	—	N.C.	—	GND connectable
134	M12	—	—	N.C.	—	GND connectable
135	N1	—	—	N.C.	—	GND connectable
136	N2	—	—	N.C.	—	GND connectable
137	N3	O	D	DMOM3	CSI-2 output	
138	N4	O	D	DMOM1	CSI-2 output	
139	N5	GND	D	VSSLIF	1.2 V GND	
140	N6	O	D	DMCKM	CSI-2 output	

No.	Pin No	I/O	A/D	Symbol	Description	Remarks
141	N7	GND	D	VSSLIF	1.2 V GND	
142	N8	O	D	DMOM2	CSI-2 output	
143	N9	O	D	DMOM4	CSI-2 output	
144	N10	O	D	DMOM5	CSI-2 output	
145	N11	—	—	N.C.	—	GND connectable
146	N12	—	—	N.C.	—	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Analog1	VDDSUB VDDHCP VDDHDA VDDHCM	AV_{DD1}		2.80	2.90	3.00	V
	Analog2	VDDHPX	AV_{DD2}		2.80	2.90	3.00	V
	Interface	VDDMIO	OV_{DD}		1.70	1.80	1.90	V
	Digital1	VDDLCN VDDLSC VDDLPL1	DV_{DD1}		1.10	1.20	1.30	V
	Digital2	VDDLPL2 VDDLPL3 VDDLIF	DV_{DD2}		1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER XTRIG SLAMODE0,1 SDA SCL TEST2	VIH	XVS / XHS Slave Mode	$0.8OV_{DD}$	—	—	V
			VIL		—	—	$0.2OV_{DD}$	V
Digital output voltage		XHS XVS TOUT TEST1	VOH	XVS / XHS Master Mode	OV_{DD}-0.2	—	—	V
			VOL		—	—	0.2	V

Current Consumption

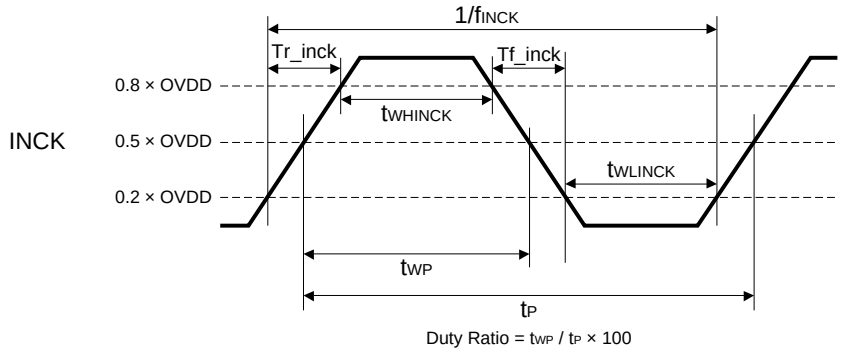
Item	Symbol	Typ.		Max.		Unit
		Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current MIPI CSI-2 / 8 Lane 12 bit, 60 frame/s All-pixel scan mode	I_{AVDD1}	38	37	51	50	mA
	I_{AVDD2}	33	32	48	47	mA
	I_{OVDD}	1	1	1	1	mA
	I_{DVDD1}	190	205	303	318	mA
	I_{DVDD2}	58	58	87	87	mA
Standby current	I_{AVDD1_STB}	—		0.1		mA
	I_{AVDD2_STB}	—		0.1		mA
	I_{OVDD_STB}	—		0.1		mA
	I_{DVDD1_STB}	—		19.8		mA
	I_{DVDD2_STB}	—		5.2		mA

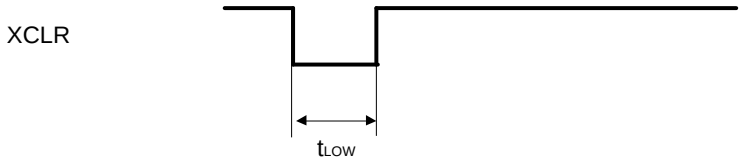
Operating current: (Typ.) Supply voltage 2.90 V / 1.8 V / 1.2 V, Tj = 25 ˚C
(Max.) Supply voltage 3.00 V / 1.9 V / 1.3 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption,
Standby: (Max.) Supply voltage 3.00 V / 1.9 V / 1.3 V, Tj = 60 ˚C, INCK: 0 V, light-obstructed state.

Standard luminous intensity: luminous intensity at 1/3 of the sensor saturated
Saturated luminous intensity: luminous intensity when the sensor is saturated.

AC Characteristics

Master Clock Waveform (INCK)





INCK 37.125MHz, 74.25MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	

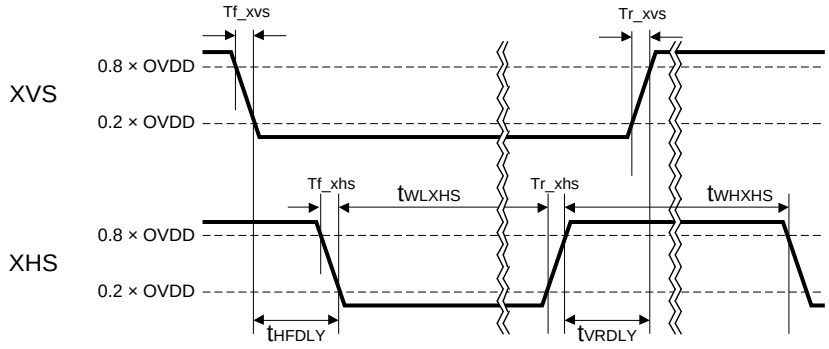
*The INCK fluctuation affects the frame rate.

INCK 6 to 27MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	6	—	27	MHz	f_{INCK} = 6 to 27MHz
INCK Low level pulse width	t_{WLINCK}	5	—	—	ns	f_{INCK} = 6 to 27MHz
INCK High level pulse width	t_{WHINCK}	5	—	—	ns	f_{INCK} = 6 to 27MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	

*The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics In Slave Mode (XMASTER pin = High)



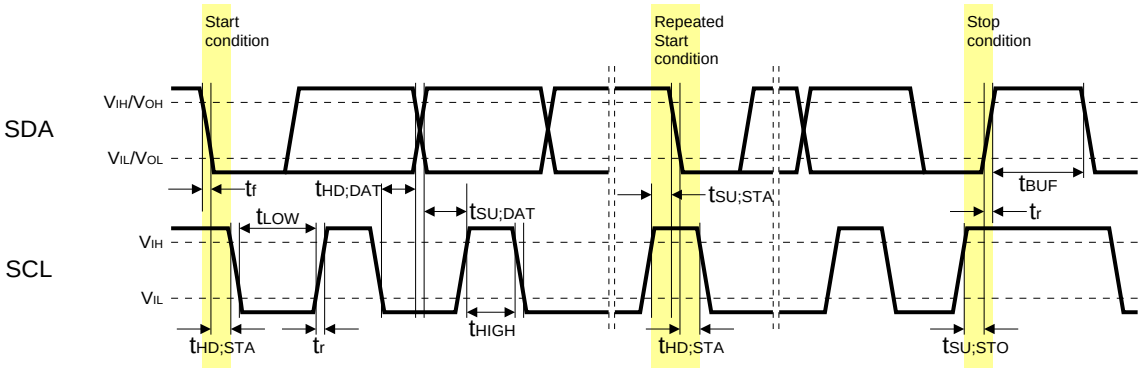
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	0	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	
XVS Rise time	T_{r_xvs}	—	—	5	ns	20 % to 80 %
XVS Fall time	T_{f_xvs}	—	—	5	ns	80 % to 20 %
XHS Rise time	T_{r_xhs}	—	—	5	ns	20 % to 80 %
XHS Fall time	T_{f_xhs}	—	—	5	ns	80 % to 20 %

XVS / XHS Input Characteristics In Master Mode (XMASTER pin = Low)

* XVS and XHS cannot be used for the sync signal to pixels.
  Be sure to detect sync code to detect the start of effective pixels in 1 line.
  For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

Serial Communication

I²C



I²C Specification

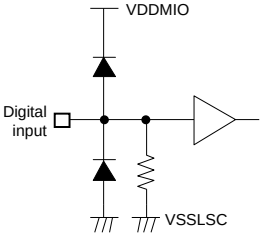
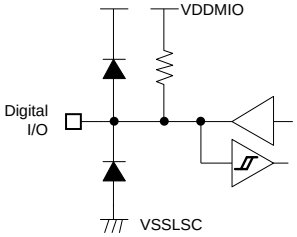
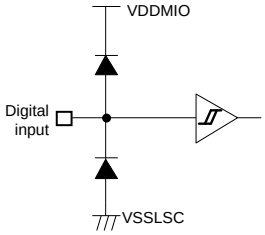
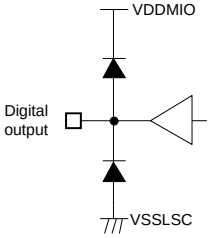
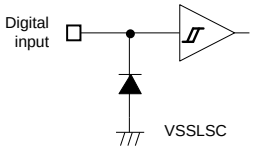
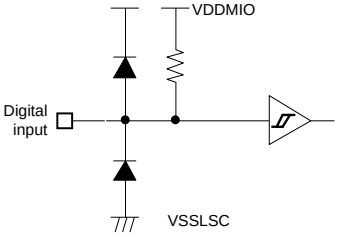
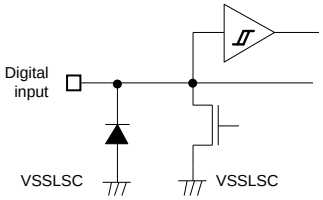
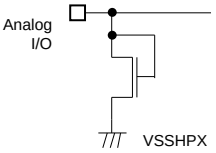
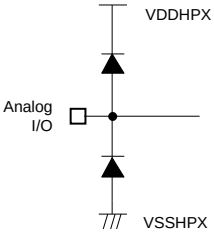
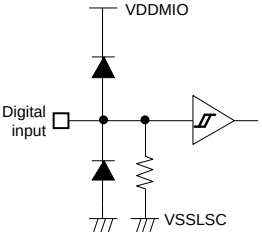
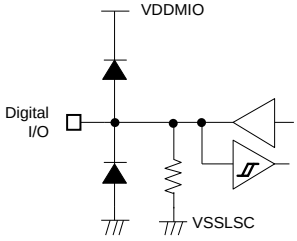
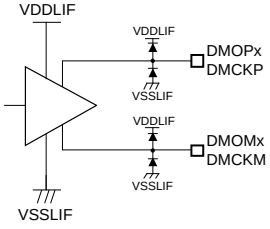
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Low level input voltage	V_{IL}	-0.3	—	0.3 × OV_{DD}	V	
High level input voltage	V_{IH}	0.7 × OV_{DD}	—	1.9	V	
Low level output voltage	V_{OL}	0	—	0.2 × OV_{DD}	V	OVDD < 2 V, Sink 3 mA
High level output voltage	V_{OH}	0.8 × OV_{DD}	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OV_{DD} – 0.3 × OV_{DD}
Input current	Ii	-10	—	10	µA	0.1 × OV_{DD} – 0.9 × OV_{DD}
Input Capacitance for SCL / SDA	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	µs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	µs

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
TENABLE		XVS XHS	
XMASTER TEST2		TEST1	
XCLR INCK		XTRIG	
SDA SCL		VRLS VRLT	
VLOADLM VBGR ASMON		SLAMODE0 SLAMODE1	
TOUT		DMOPx DMOMx DMCKP DMCKM	

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

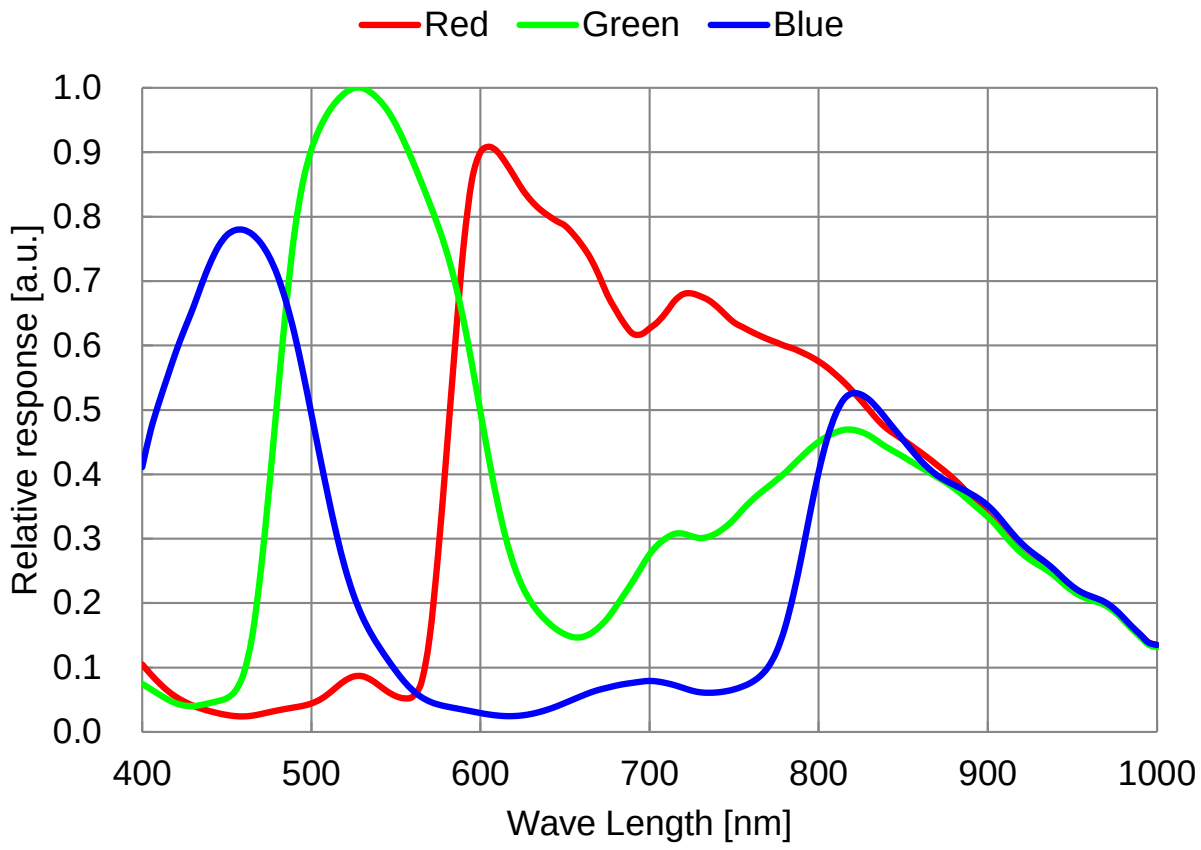


Image Sensor Characteristics

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, All-pixel scan mode, 12 bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	1870 (429)	2200 (505)	—	Digit (mV)	1	1/30 s storage 12 bit converted value
Sensitivity ratio	R / G	RG	0.42	—	0.58	—	2	—
	B / G	BG	0.31	—	0.48	—		
Saturation signal		Vsat	3895 (894)	—	—	Digit (mV)	3	12 bit converted value
Video signal shading		SH	—	—	25	%	4	—
Vertical line		VL	—	—	90	µV	5	12 bit converted value’
Dark signal		Vdt	—	—	0.57 (0.13)	Digit (mV)	6	1/30 s storage 12 bit converted value
Dark signal shading		ΔVdt	—	—	0.57 (0.13)	Digit (mV)	7	1/30 s storage 12 bit converted value

Note) 1. Converted value into mV using 1Digit = 0.2295 mV for 12-bit output and 1Digit = 0.9180 mV for 10-bit output.

2. The video signal shading is the measured value in the wafer status (including color filter) and does not include characteristics of the seal glass.

3. The characteristics above apply to effective pixel area that is shown below.

Zone Definition

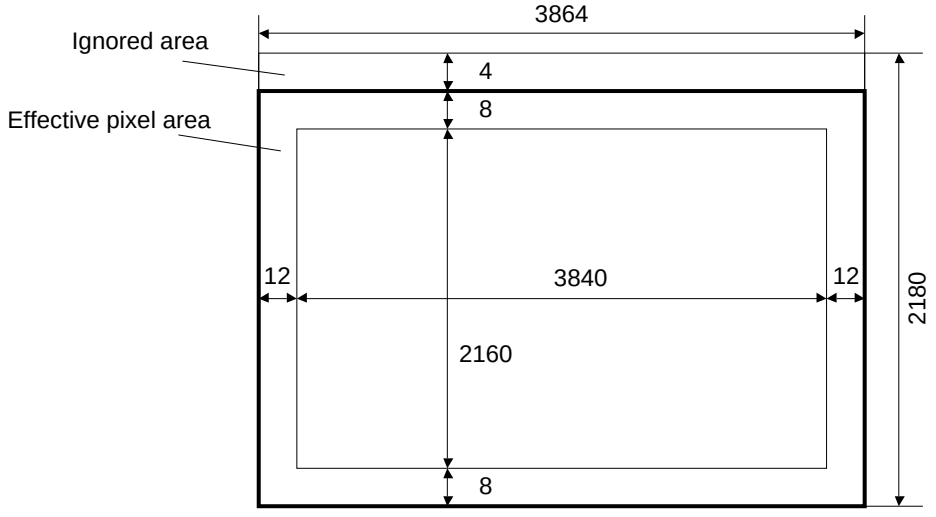


Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr / Gb channel signal output or the R / B channel signal output of the measurement system.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance - 30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   S = (VGr + VGb) / 2 × 100/30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 505 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signa l
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 505 mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 505 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   SH = (Gmax – Gmin) / 505 × 100 [%]

5. Vertical Line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculates each average output of Gr, Gb, R and B on respective columns. Calculates maximum value of difference with adjacent column on the same color (VL [µV]).

6. Dark signal
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

7. Dark signal shading
   After the measurement item 6, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

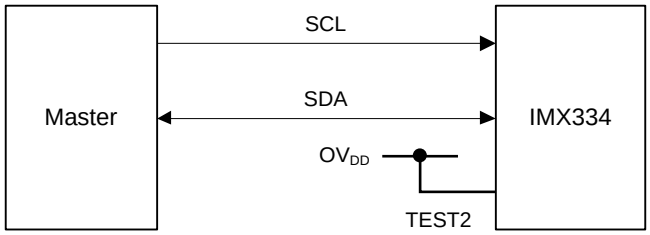
   ΔVdt = Vdmax – Vdmin [mV]

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by I^2C communication. See the Register Map for the addresses and setting values to be set.

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions. Using SLAMODE0 and SLAMODE1 pins , SLAVE address can be changed.



Pin connection of serial communication

SLAVE Address

SLAMODE1 pin	SLAMODE0 pin	MSB							LSB
Low	Low	0	0	1	1	0	1	0	R / W
Low	High	0	0	1	0	0	0	0	R / W
High	Low	0	1	1	0	1	1	0	R / W
High	High	0	1	1	0	1	1	1	R / W

* R/W is data direction bit

R / W

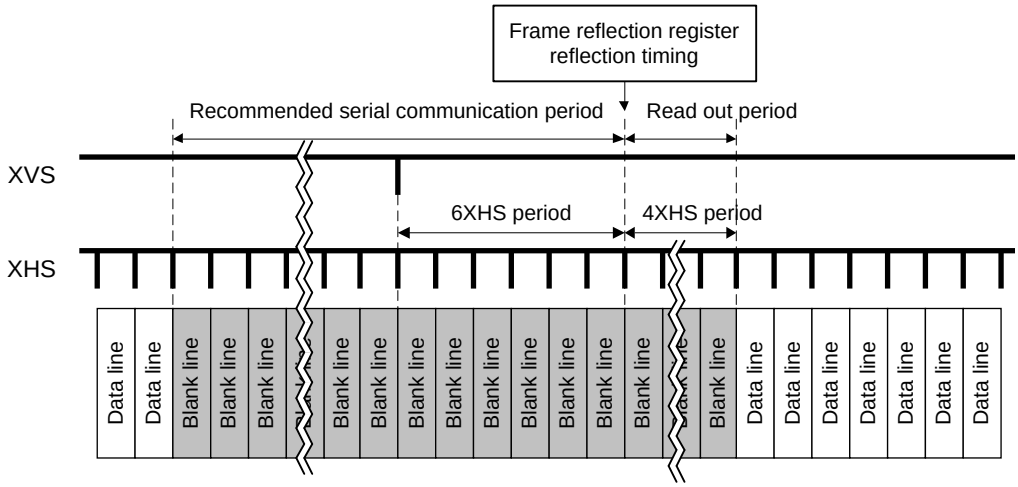
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Remarks
SCL	E3	I^2C serial clock input
SDA	D1	I^2C serial data communication

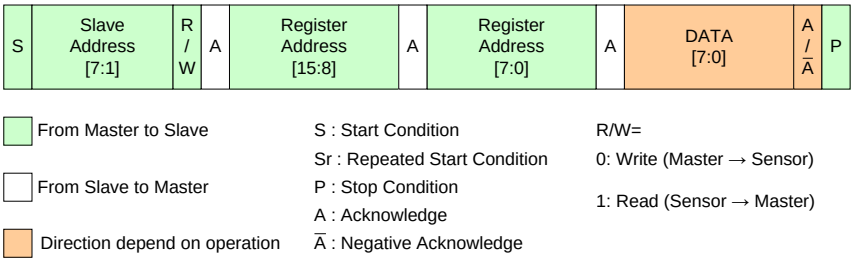
Register Communication Timing (I^2C)

In I^2C communication system, communication can be performed during the falling edge of XVS to 6H. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.) Using REGHOLD function is recommended for register setting using I^2C communication. For REGHOLD function, see “Register Transmission Setting” in “Description of Functions”.



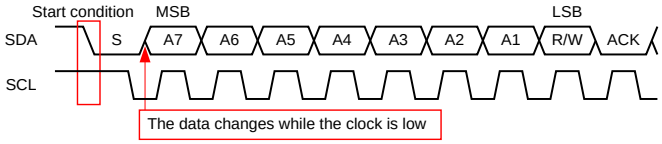
Communication Protocol

I^{2}C serial communication supports a 16-bit register address and 8-bit data message type.

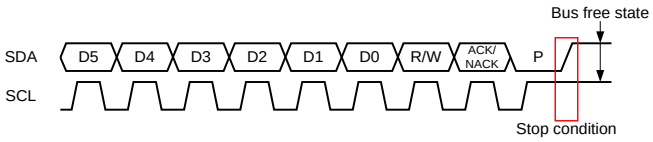


Communication Protocol

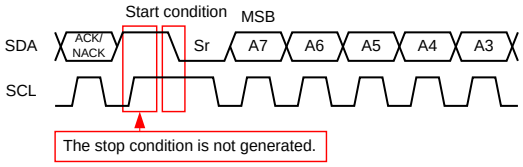
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

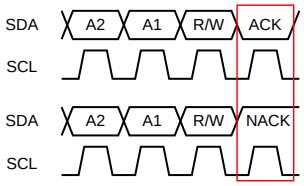


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



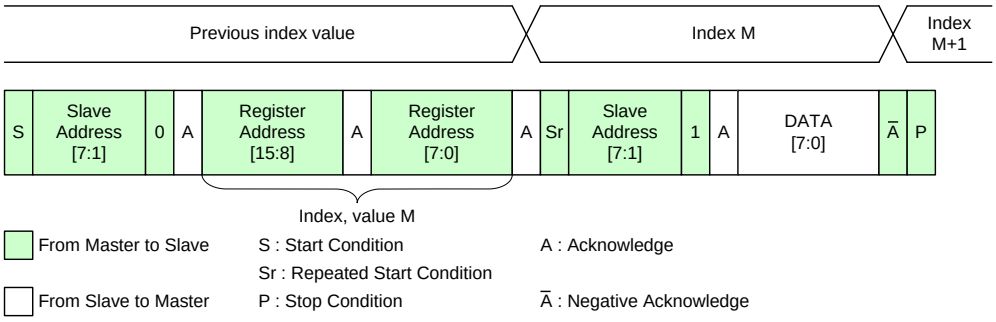
Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

This sensor corresponds to four reed modes and the two write modes.

Single Read from Random Location

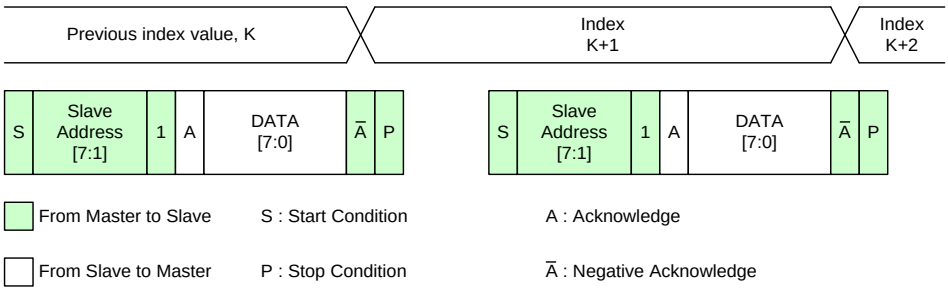
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

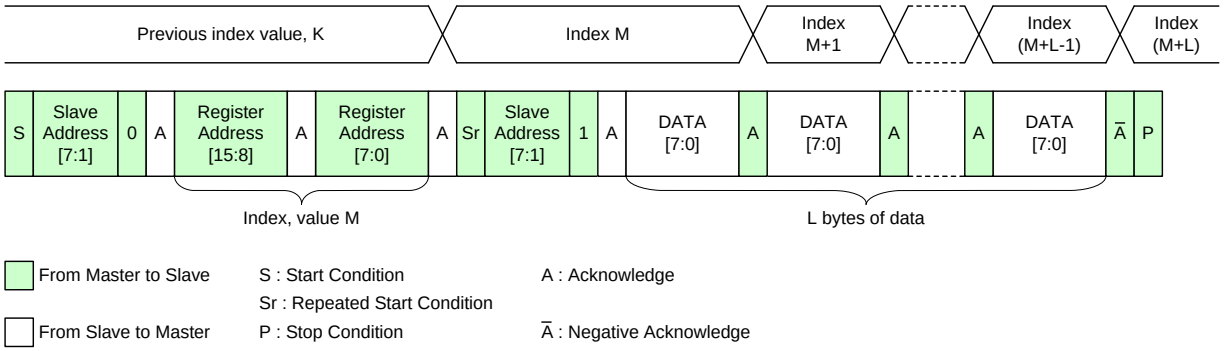
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

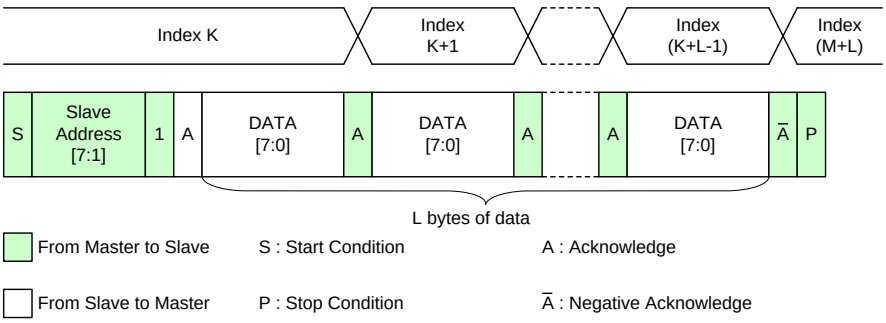
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

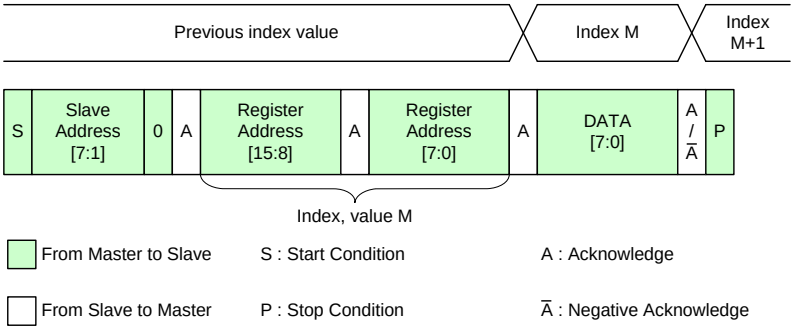
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

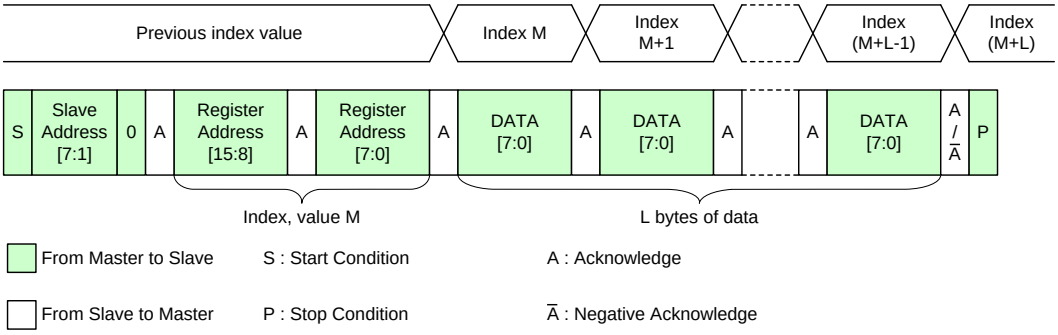
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 4096 bytes (256 × 16) of registers, composed of registers with LSB addresses 00h to FFh that correspond to MSB address 30h to 3Fh. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 4096 bytes.

The values must be changed from the default value, so initial setting after reset is required after power-on. There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than belows, set them in sensor standby state.

STANDBY
REGHOLD
XMSTA
XVSOUTSEL [1:0]
XHSOUTSEL [1:0]

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for LSB address; 3000h to 3FFFh.

* For the register that is writing " * " to the setting value in description (Indicated by red letter), change the value from the default value after the reset.

** In Gain setting only, it is reflected on the next frame which was settings.

(1) Registers corresponding to address = 30**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	Immediately
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	Immediately
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	Immediately
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3003h	[7:0]	—	Fixed to “0h”	0h	0h	—
3004h	[7:0]	RESTART	When changing from 4h to 0h : Restart Refer to the “Sensor setting flow”	0h	0h	Immediately
3005h to 300Bh	[7:0]	—	Reserved	—	—	—
300Ch	0	BCWAIT_TIME	The value is set according to INCK. Refer to “INCK setting”	B6h	B6h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
300Dh	0 1 2 3 4 5 6 7	CPWAIT_TIME	The value is set according to INCK. Refer to “INCK setting”	7Fh	7Fh	Immediately
300Eh to 3017h	[7:0]	—	Reserved	—	—	—
3018h	0 1 2 3	WINMODE [3:0]	Window mode setting 0: All-pixel scan mode 1: Horizontal/Vertical 2/2-line binning 4: Window cropping mode Others: Setting prohibited	0h	00h	V
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3019h to 302Bh	[7:0]	—	Reserved	—	—	—
302Ch	0 1 2 3 4 5 6 7	HTRIMMING_START [11:0]	LSB In window cropping mode Start position (Horizontal direction)	030h	30h	V
302Dh	0 1 2 3		 MSB		00h	
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
302Eh	0	HNUM [11:0]	LSB In window cropping mode Cropping sizes designation (Horizontal direction)	F18h	18h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
302Fh	0				0Fh	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3030h	0	VMAX [19:0]	LSB When sensor master mode vertical span setting. For details, see the item of “Slave Mode and Master Mode” In the section of “Description of Various Functions”	0008CAh	CAh	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3031h	0				08h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3032h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3033h	[7:0]	—	Fixed to “0h”	00h	00h	—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3034h	0	HMAX [15:0]	LSB	0226h	26h	V
	1					
	2					
	3					
	4					
	5		When sensor master mode horizontal span setting.			
	6					
	7		For details, see the item of “Slave Mode and Master Mode” In the section of “Description of Various Functions”			
3035h	0				02h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
3036h to 304Bh	[7:0]	—	Reserved	—	—	—
304Ch	0	OPB_SIZE_V [5:0]	LSB	14h	14h	V
	1					
	2					
	3		Vertical direction OB width setting.			
	4					
	5		MSB			
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
304Dh	[7:0]	—	Reserved	—	—	—
304Eh	0	HREVERSE	Horizontal direction Readout inversion control 0: Normal 1: Inverted	0h	00h	V
	1		Fixed to “0h”	0h		—
	2		Fixed to “0h”	0h		—
	3		Fixed to “0h”	0h		—
	4		Fixed to “0h”	0h		—
	5		Fixed to “0h”	0h		—
	6		Fixed to “0h”	0h		—
	7		Fixed to “0h”	0h		—
304Fh	0	VREVERSE	Vertical direction 0: Normal 1: Inverted	0h	00h	V
	1		Fixed to “0h”	0h		—
	2		Fixed to “0h”	0h		—
	3		Fixed to “0h”	0h		—
	4		Fixed to “0h”	0h		—
	5		Fixed to “0h”	0h		—
	6		Fixed to “0h”	0h		—
	7		Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3050h	0	ADBIT	AD conversion bits setting 0: AD10bit 1: AD12bit	1h	01h	Immediately
	1		Fixed to “0h”	0h		—
	2		Fixed to “0h”	0h		—
	3		Fixed to “0h”	0h		—
	4		Fixed to “0h”	0h		—
	5		Fixed to “0h”	0h		—
	6		Fixed to “0h”	0h		—
	7		Fixed to “0h”	0h		—
3051h to 3057h	[7:0]	—	Reserved	—	—	—
3058h	0	SHR0 [19:0]	LSB	00005h	05h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3059h	0		Storage time adjustment Designated in line units.		00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
305Ah	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
305Bh to 3073h	[7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3074h	0	AREA3_ST_ADR_1 [12:0]	LSB In window cropping mode Designation of upper left coordinate for cropping position (Vertical position)	00B0h	B0h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3075h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3076h	0	AREA3_WIDTH_1 [12:0]	LSB In window cropping mode Cropping size designation (Vertical direction)	0884h	84h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3077h	0				08h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3078h to 308Dh	[7:0]	—	Reserved	—	—	—
308Eh	0	AREA3_ST_ADR_2 [12:0]	LSB In window cropping mode set to “AREA3_ST_ADR_1 + 1”	00B1h	B1h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
308Fh	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3090h	0	AREA3_WIDTH_2 [12:0]	LSB In window cropping mode Cropping size designation (Vertical direction)	0884h	84h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3091h	0				08h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
3092h to 30B5h	[7:0]	—	Reserved	—	—	—
30B6h	0	UNREAD_PARAM5 [8:0]	LSB In window cropping mode	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
30B7h	0		MSB		00h	
	1	—	Fixed to “0h”	0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	—	Fixed to “0h”	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
30B8h to 30C5h	[7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30C6h	0	BLACK_OFSET_ADR [12:0]	LSB	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6		In window cropping mode setting			
	7					
30C7h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
30C8h to 30CDh	[7:0]	—	Reserved	—	—	—
30CEh	0	UNRD_LINE_MAX [12:0]	LSB	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6		In window cropping mode setting			
	7					
30CFh	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
30D0h to 30D7h	[7:0]	—	Reserved	—	—	—
30D8h	0	UNREAD_ED_ADR [12:0]	LSB	11F8h	F8h	V
	1					
	2					
	3					
	4					
	5					
	6		In window cropping mode setting			
	7					
30D9h	0				11h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30DAh to 30E7h	[7:0]	—	Reserved	—	—	—
30E8h	0	GAIN [10:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4					
	5		Gain setting (0.0dB to 72.0dB / 0.3dB step)			
	6					
	7					
30E9h	0				00h	
	1					
	2		MSB			
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30EAh to 30FFh	[7:0]	—	Reserved	—	—	—

(2) Registers corresponding to address = 31**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3100h to 3115h	[7:0] to [7:0]	—	Reserved	—	—	—
3116h	0	UNREAD_PARAM6 [8:0]	LSB	0008h	08h	V
	1					
	2					
	3					
	4		In window cropping mode ssetting			
	5					
	6					
	7					
3117h	0		MSB		00h	
	1	—	Fixed to “0h”	0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	—	Fixed to “0h”	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
3118h to 314Bh	[7:0] to [7:0]	—	Reserved	—	—	—
314Ch	0	INCKSEL1 [8:0]	LSB	0C0h	C0h	Immediately
	1					
	2					
	3					
	4		The value is set according to INCK. Refer to “INCK setting”			
	5					
	6					
	7					
314Dh	0		MSB		00h	
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
314Eh to 3159h	[7:0] to [7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
315Ah	0	INCKSEL2 [1:0]	The value is set according to INCK. Refer to “INCK setting”	3h	03h	Immediately
	1					
	2	PLL_IF_GC [1:0]		0h		
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
315Bh to 3167h	[7:0] to [7:0]	—	Reserved	—	—	—
3168h	0	INCKSEL3 [7:0]	The value is set according to INCK. Refer to “INCK setting”	68h	68h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3169h	[7:0]	—	Reserved	—	—	—
316Ah	0	INCKSEL4 [1:0]	The value is set according to INCK. Refer to “INCK setting”	3h	7Fh	Immediately
	1					
	2	—	Fixed to “1h”	1h		
	3	—	Fixed to “1h”	1h		
	4	—	Fixed to “1h”	1h		
	5	—	Fixed to “1h”	1h		
	6	—	Fixed to “1h”	1h		
	7	—	Fixed to “0h”	0h		
316Bh to 3198h	[7:0] to [7:0]	—	Reserved	—	—	—
3199h	0	—	Fixed to “0h”	0h	00h	Immediately
	1	—	Fixed to “0h”	0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	HADD	Mode setting 0: All-pixel scan mode 3: Horizontal/Vertical 2/2-line binning	0h		
	5	VADD		0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
319Ah to 319Ch	[7:0] to [7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
319Dh	0	MDBIT	Number of output bit setting 0: 10 bit 1: 12bit	1h	01h	V
	1	—	Fixed to “0h”	0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	—	Fixed to “0h”	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
319Eh	0	SYS_MODE	The value is set according to INCK. Refer to “INCK setting”	0h	00h	Immediately
	1					
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	—	Fixed to “0h”	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
319Fh	[7:0]	—	Reserved	—	—	—
31A0h	0	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Fixed to Low 2: VSYNC output	2h	2Ah	Immediately
	1					
	2	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Fixed to Low 2: HSYNC output	2h		
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “1h”	1h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
31A1h	0	XVS_DRV [1:0]	XVS pin setting 0: XVS output (Master mode) 3: HiZ (Slave mode)	3h	0Fh	Immediately
	1					
	2	XHS_DRV [1:0]	XHS pin setting 0: XHS output (Master mode) 3: HiZ (Slave mode)	3h		
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
31A2h to 31D3h	[7:0] to [7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
31D4h	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XVSLNG [1:0]	XVS pulse width setting in master mode. 0: 1H 1: 2H 2: 4H 3: 8H	0h		Immediately
	5					
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
31D5h	0	—	Fixed to “0h”	0h	00h	—
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	XHSLNG [1:0]	XHS pulse width setting in master mode. 0: 16clock 1: 32clock 2: 64clock 3: 128clock	0h		Immediately
	5			0h		
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
31D6h to 31DCh	[7:0] to [7:0]	—	Reserved	—	—	—
31DDh	0	VALID_EXPAND [2:0]	Mode setting 3: All-pixel scan mode 4: Horizontal/Vertical 2/2-line binning	1h	03h	Immediately
	1			1h		
	2			0h		
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
31DEh to 31FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(3) Registers corresponding to address = 32**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3200h to 3287h	[7:0] to [7:0]	—	Reserved	—	—	—
3288h	[7:0]	—	Set to “21h”	20h	20h	Immediately
3289h	[7:0]	—	Reserved	—	—	—
328Ah	[7:0]	—	Set to “02h”	03h	03h	Immediately
328Bh to 32FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(4) Registers corresponding to address = 33**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3300h	0	TCYCLE [1:0]	Mode setting 0: All-pixel scan mode 1: Horizontal/Vertical 2/2-line binning	0h	00h	Immediately
	1					
	2		Fixed to “0h”	0h		
	3		Fixed to “0h”	0h		
	4		Fixed to “0h”	0h		
	5		Fixed to “0h”	0h		
	6		Fixed to “0h”	0h		
	7		Fixed to “0h”	0h		
3301h	[7:0]	—	Reserved	—	—	—
3302h	0	BLKLEVEL [9:0]	LSB	032h	32h	Immediately
	1					
	2					
	3		Black level offset value setting			
	4					
	5		10-bit readout mode: 1digit/1h 12-bit readout mode: 4digit/1h			
	6					
	7					
3303h	0				00h	
	1		MSB			
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3304h to 3307h	[7:0] to [7:0]	—	Reserved	—	—	—
3308h	0	Y_OUT_SIZE [12:0]	LSB	884h	84h	V
	1					
	2					
	3					
	4					
	5					
	6		Set the number of effective pixel lines			
	7					
3309h	0				08h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
330Ah to 33FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(5) Registers corresponding to address = 34**h.

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
3400h to 3413h	[7:0] to [7:0]	—	Reserved	—	—	—
3414h	[7:0]	—	Set to “05h”	0Ah	0Ah	Immediately
3415h	[7:0]	—	Reserved	—	—	—
3416h	[7:0]	—	Set to “18h”	04h	04h	Immediately
3417h to 341Bh	[7:0] to [7:0]	—	Reserved	—	—	—
341Ch	0	ADBIT1 [8:0]	LSB The value is set according to AD Conversion bits 10-bit : 1FFh 12-bit : 047h	047h	47h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					
341Dh	0		MSB		00h	
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
341Eh to 34FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(6) Registers corresponding to address = 35**h.

Address	bit	Register name	Description	Default value after reset		Default value after reset
				By register	By address	
3500h to 35ABh	[7:0] to [7:0]	—	Reserved	—	—	—
35ACh	[7:0]	—	Set to “0Eh”	12h	12h	Immediately
35ADh to 35FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(7) Registers corresponding to address = 36**h.

Address	bit	Register name	Description	Default value after reset		Default value after reset
				By register	By address	
3600h to 3647h	[7:0] to [7:0]	—	Reserved	—	—	—
3648h	[7:0]	—	Set to “01h”	10h	10h	Immediately
3649h	[7:0]	—	Reserved	—	—	—
364Ah	[7:0]	—	Set to “04h”	0Ah	0Ah	Immediately
364Bh	[7:0]	—	Reserved	—	—	—
364Ch	[7:0]	—	Set to “04h”	00h	00h	Immediately
364Dh to 3677h	[7:0] to [7:0]	—	Reserved	—	—	—
3678h	[7:0]	—	Set to “01h”	00h	00h	Immediately
3679h to 367Bh	[7:0] to [7:0]	—	Reserved	—	—	—
367Ch	[7:0]	—	Set to “31h”	1Eh	1Eh	Immediately
367Dh	[7:0]	—	Reserved	—	—	—
367Eh	[7:0]	—	Set to “31h”	1Eh	1Eh	Immediately
367Fh to 36FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(8) Registers corresponding to address = 37**h.

Address	bit	Register name	Description	Default value after reset		Default value after reset
				By register	By address	
3700h to 3707h	[7:0] to [7:0]	—	Reserved	—	—	—
3708h	[7:0]	—	Set to “02h”	00h	00h	Immediately
3709h to 3713h	[7:0] to [7:0]	—	Reserved	—	—	—
3714h	[7:0]	—	Set to “01h”	00h	00h	Immediately
3715h	[7:0]	—	Set to “02h”	00h	00h	Immediately
3716h	[7:0]	—	Set to “02h”	00h	00h	Immediately
3717h	[7:0]	—	Set to “02h”	00h	00h	Immediately
3718h to 371Bh	[7:0] to [7:0]	—	Reserved	—	—	—
371Ch	[7:0]	—	Set to “3Dh”	3Eh	3Eh	Immediately
371Dh	[7:0]	—	Set to “3Fh”	01h	01h	Immediately
371Eh to 372Bh	[7:0] to [7:0]	—	Reserved	—	—	—
372Ch	[7:0]	—	Set to “00h”	46h	46h	Immediately
372Dh	[7:0]	—	Set to “00h”	01h	01h	Immediately
372Eh	[7:0]	—	Set to “46h”	58h	58h	Immediately
372Fh	[7:0]	—	Set to “00h”	02h	02h	Immediately
3730h	[7:0]	—	Set to “89h”	00h	00h	Immediately
3731h	[7:0]	—	Set to “00h”	04h	04h	Immediately
3732h	[7:0]	—	Set to “08h”	2Ch	2Ch	Immediately
3733h	[7:0]	—	Set to “01h”	05h	05h	Immediately
3734h	[7:0]	—	Set to “FEh”	00h	00h	Immediately
3735h	[7:0]	—	Set to “05h”	06h	06h	Immediately
3736h to 375Ch	[7:0] to [7:0]	—	Reserved	—	—	—
375Dh	[7:0]	—	Set to “00h”	74h	74h	Immediately
375Eh	[7:0]	—	Set to “00h”	B9h	B9h	Immediately
375Fh	[7:0]	—	Set to “61h”	CBh	CBh	Immediately
3760h	[7:0]	—	Set to “06h”	0Ch	0Ch	Immediately
3761h to 3767h	[7:0] to [7:0]	—	Reserved	—	—	—
3768h	[7:0]	—	Set to “1Bh”	0Dh	0Dh	Immediately
3769h	[7:0]	—	Set to “1Bh”	0Dh	0Dh	Immediately
376Ah	[7:0]	—	Set to “1Ah”	0Dh	0Dh	Immediately
376Bh	[7:0]	—	Set to “19h”	0Dh	0Dh	Immediately
376Ch	[7:0]	—	Set to “18h”	0Dh	0Dh	Immediately
376Dh	[7:0]	—	Set to “14h”	0Dh	0Dh	Immediately
376Eh	[7:0]	—	Set to “0Fh”	0Dh	0Dh	Immediately
376Fh to 3775h	[7:0] to [7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset		Default value after reset
				By register	By address	
3776h	[7:0]	—	Set to “00h”	58h	58h	Immediately
3777h	[7:0]	—	Set to “00h”	02h	02h	Immediately
3778h	[7:0]	—	Set to “46h”	00h	00h	Immediately
3779h	[7:0]	—	Set to “00h”	04h	04h	Immediately
377Ah	[7:0]	—	Set to “08h”	80h	80h	Immediately
377Bh	[7:0]	—	Set to “01h”	05h	05h	Immediately
377Ch	[7:0]	—	Set to “45h”	96h	96h	Immediately
377Dh	[7:0]	—	Set to “01h”	06h	06h	Immediately
377Eh	[7:0]	—	Set to “23h”	4Ah	4Ah	Immediately
377Fh	[7:0]	—	Set to “02h”	07h	07h	Immediately
3780h	[7:0]	—	Set to “D9h”	80h	80h	Immediately
3781h	[7:0]	—	Set to “03h”	07h	07h	Immediately
3782h	[7:0]	—	Set to “F5h”	A6h	A6h	Immediately
3783h	[7:0]	—	Set to “06h”	07h	07h	Immediately
3784h	[7:0]	—	Set to “A5h”	B8h	B8h	Immediately
3785h to 3787h	[7:0] to [7:0]	—	Reserved	—	—	—
3788h	[7:0]	—	Set to “0Fh”	09h	09h	Immediately
3789h	[7:0]	—	Reserved	—	—	—
378Ah	[7:0]	—	Set to “D9h”	58h	58h	Immediately
378Bh	[7:0]	—	Set to “03h”	02h	02h	Immediately
378Ch	[7:0]	—	Set to “EBh”	00h	00h	Immediately
378Dh	[7:0]	—	Set to “05h”	04h	04h	Immediately
378Eh	[7:0]	—	Set to “87h”	80h	80h	Immediately
378Fh	[7:0]	—	Set to “06h”	05h	05h	Immediately
3790h	[7:0]	—	Set to “F5h”	96h	96h	Immediately
3791h	[7:0]	—	Reserved	—	—	—
3792h	[7:0]	—	Set to “43h”	4Ah	4Ah	Immediately
3793h	[7:0]	—	Reserved	—	—	—
3794h	[7:0]	—	Set to “7Ah”	80h	80h	Immediately
3795h	[7:0]	—	Reserved	—	—	—
3796h	[7:0]	—	Set to “A1h”	A6h	A6h	Immediately
3797h to 37AFh	[7:0] to [7:0]	—	Reserved	—	—	—
37B0h	[7:0]	—	XMASTER pin High : Set to “37h” XMASTER pin Low : Set to “36h”	36h	36h	Immediately
37B1h to 37FFh	[7:0] to [7:0]	—	Reserved	—	—	—

(9) Registers corresponding to address = 3A**h.

Address	bit	Register name	Description	Default value		Reflection timing
				By register	By address	
3A00h	[7:0]	—	Reserved	—	—	—
3A01h	0 1 2	LANEMODE [2:0]	Output interface selection 3: CSI-2 4lane 7: CSI-2 8lane Others: Setting prohibited	3h	03h	Immediately
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3A02h to 3A17h	[7:0] to [7:0]	—	Reserved	—	—	—
3A18h	[7:0]	TCLKPOST [15:0]	Global timing setting	00B7h	B7h	Immediately
3A19h	[7:0]				00h	
3A1Ah	[7:0]	TCLKPREPARE [15:0]	Global timing setting	0067h	67h	Immediately
3A1Bh	[7:0]				00h	
3A1Ch	[7:0]	TCLKTRAIL [15:0]	Global timing setting	006Fh	6Fh	Immediately
3A1Dh	[7:0]				00h	
3A1Eh	[7:0]	TCLKZERO [15:0]	Global timing setting	01DFh	DFh	Immediately
3A1Fh	[7:0]				01h	
3A20h	[7:0]	THSPREPARE [15:0]	Global timing setting	006Fh	6Fh	Immediately
3A21h	[7:0]				00h	
3A22h	[7:0]	THSZERO [15:0]	Global timing setting	00CFh	CFh	Immediately
3A23h	[7:0]				00h	
3A24h	[7:0]	THSTRAIL [15:0]	Global timing setting	006Fh	6Fh	Immediately
3A25h	[7:0]				00h	
3A26h	[7:0]	THSEXIT [15:0]	Global timing setting	00B7h	B7h	Immediately
3A27h	[7:0]				00h	
3A28h	[7:0]	TLPX[15:0]	Global timing setting	005Fh	5Fh	Immediately
3A29h	[7:0]				00h	
3A30h to 3AFFh	[7:0] to [7:0]	—	Reserved	—	—	—

(10) Registers corresponding to address = 3E**h.

Address	bit	Register name	Description	Default value		Reflection timing
				By register	By address	
3E00h to 3E03h	[7:0] to [7:0]	—	Reserved	—	—	—
3E04h	[7:0]	—	Set to “0Eh”	12h	12h	Immediately
3E05h to 3EFFh	[7:0] to [7:0]	—	Reserved	—	—	—

Readout Drive mode

Operating mode

The table below lists the operating modes available with this sensor. (N/A: Not supported mode)

Mode	INCK [MHz]	Recording Pixels		AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Data rate [Mbps/Lane]		1H period [μs]	
							CSI-2		CSI-2	
		H [pixels]	V [lines]				4 Lane	8 Lane	4 Lane	8 Lane
All pixel	6-27 37.125 74.25	3840	2160	10	10	30 / 25	891/1188	891/1188	14.81	14.81
				10	10	60 / 50	1782	891/1188	7.41	7.41
				12	12	30 / 25	891/1188	891/1188	14.81	14.81
				12	12	60 / 50	1782	891/1188	7.41	7.41
Horizontal/ Vertical 2/2-line binning	6-27 37.125 74.25	1920	1080	10	12	30 / 25	891/1188	891/1188	29.63	29.63
				10	12	60 / 50	1188/1782	891/1188	14.81	14.81
				10	12	120	NA	1188	NA	7.41

Image Data Output Format (CSI-2 output)

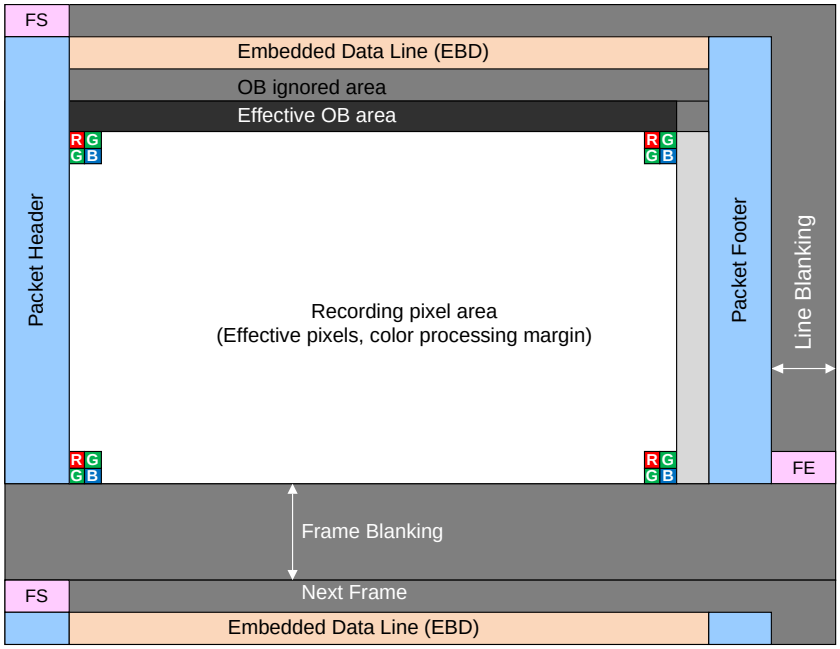
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
10h	NULL	N/A	Invalid data
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 319Dh MDBIT [0]	0A0Ah
2Ch	RAW12		0C0Ch
37h	OB Data	N/A	Vertical OB line data

Frame Structure

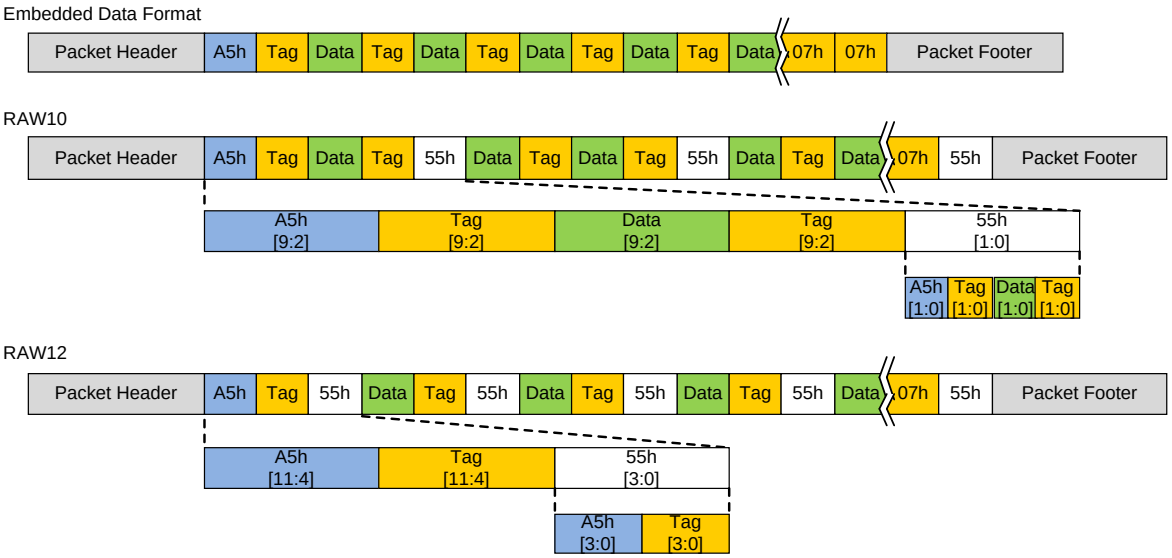


Frame Structure of CSI-2 output

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.

Embedded Data Format



The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data.
07h	End of Data.
AAh	CCI Register Index MSB [15:8]
A5h	CCI Register Index LSB [7:0]
5Ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
FFh	Illegal Tag. If found treat as end of Data.

Specific output examples are shown below.

Output timing	bit	Transfer data	Description
E00 to E01	[7:0]	–	ignored
E02	[2:0]	–	ignored
	[3]	HREVERSE	
	[7:4]	–	ignored
E03 to E07	[7:0]	–	ignored
E08	[4:0]	–	ignored
	[5]	VREVERSE	
	[7:6]	–	ignored
E09	[7:0]	–	ignored
E10	[6:0]	–	ignored
	[7]	ADBIT	
E11	[7:0]	–	ignored
E12	[3:0]	–	ignored
	[5:4]	MDBIT	
	[7:6]	–	ignored
E13 to E14	[7:0]	–	ignored
E15	[7:0]	GAIN	
E16	[2:0]		
	[7:3]	–	ignored
E17 to E22	[7:0]	–	ignored
E23	[7:0]	SHR0	
E24	[7:0]		
E25	[3:0]		
	[7:4]	–	ignored
E26 to E52	[7:0]	–	ignored
E53	[7:0]	BLKLEVEL	
E54	[1:0]		
	[7:2]	–	ignored
E55 to E191	[7:0]	–	ignored

Image Data Output Format

All-pixel scan mode

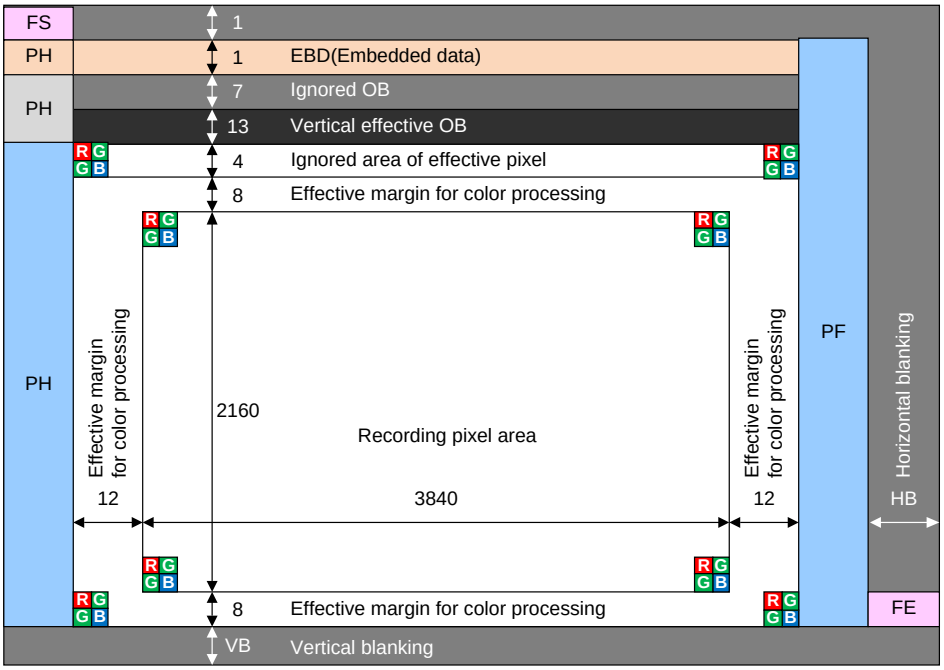
List of Setting Register

Address	bit	Register Name	Initial Value	CSI-2 serial								Remarks
				4 lane	8 lane	4lane	8lane	4 lane	8 lane	4lane	8lane	
				30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	60 / 50 [frame /s]	30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	60 / 50 [frame /s]	
AD Conversion [bit]				10	10	10	10	12	12	12	12	
Output bit width [bit]				10	10	10	10	12	12	12	12	
Data rate [Mbps/lane]				891/1188	891/1188	1782	891/1188	891/1188	891/1188	1782	891/1188	
3018h	[3:0]	WINMODE	0h	0h								
3030h	[7:0]	VMAX	08CAh	08CAh								25 /30 / 50 / 60 [frame/s]
3031h	[7:0]											
3032h	[3:0]											
3034h	[7:0]	HMAX	0226h	044Ch / 0528h	044Ch / 0528h	0226h / 0294h	0226h / 0294h	044Ch / 0528h	044Ch / 0528h	0226h / 0294h	0226h / 0294h	30 / 25 [frame / s] / 60 / 50 [frame / s]
3035h	[7:0]											
304Ch	[7:0]	OPB_SIZE_V	14h	14h								
304Eh	[7:0]	HREVERSE	00h	00h / 01h								0: Normal 1: Inverted
304Fh	[7:0]	VREVERSE	00h	00h / 01h								0: Normal 1: Inverted
3050h	[7:0]	ADBIT	01h	00h / 01h								0: 10 bit, 1: 12 bit
3074h	[7:0]	AREA3_ST_ ADR_1	00B0h	Vertical read out Normal：00B0h , Inverted：11C0h								
3075h	[4:0]											
308Eh	[7:0]	AREA3_ST_ ADR_2	00B1h	Vertical read out Normal：00B1h , Inverted：11C1h								
308Fh	[4:0]											
30B6h	[7:0]	UNREAD_ PARAM5	0000h	Vertical read out Normal：0000h , Inverted：01FAh								
30B7h	[0]											
3116h	[7:0]	UNREAD_ PARAM6	0008h	Vertical read out Normal：0008h , Inverted：0002h								
3117h	[0]											
314Ch	[7:0]	INCKSEL1	00C0h	Refer to “INCK setting”								
314Dh	[0]											
315Ah	[1:0]	INCKSEL2	3h									
	[3:2]	PLL_IF_GC	0h									
3168h	[7:0]	INCKSEL3	68h									
316Ah	[1:0]	INCKSEL4	3h									
3199h	[4]	HADD	0h	0h								
	[5]	VADD										
319Dh	[0]	MDBIT	1h	0h / 1h								0: 10 bit, 1: 12 bit
319Eh	[1:0]	SYS_MODE	0h	Refer to “INCK setting”								
31DDh	[2:0]	VALID_EXPAND	3h	3h								
3300h	[1:0]	TCYCLE	0h	0h								
3308h	[7:0]	Y_OUT_SIZE	0884h	0884h								
3309h	[4:0]											
341Ch	[7:0]	ADBIT1	0047h	10bit AD : 01FFh 12bit AD : 0047h								
341Dh	[0]											
3A01h	[2:0]	LANEMODE	3h	3h	7h	3h	7h	3h	7h	3h	7h	

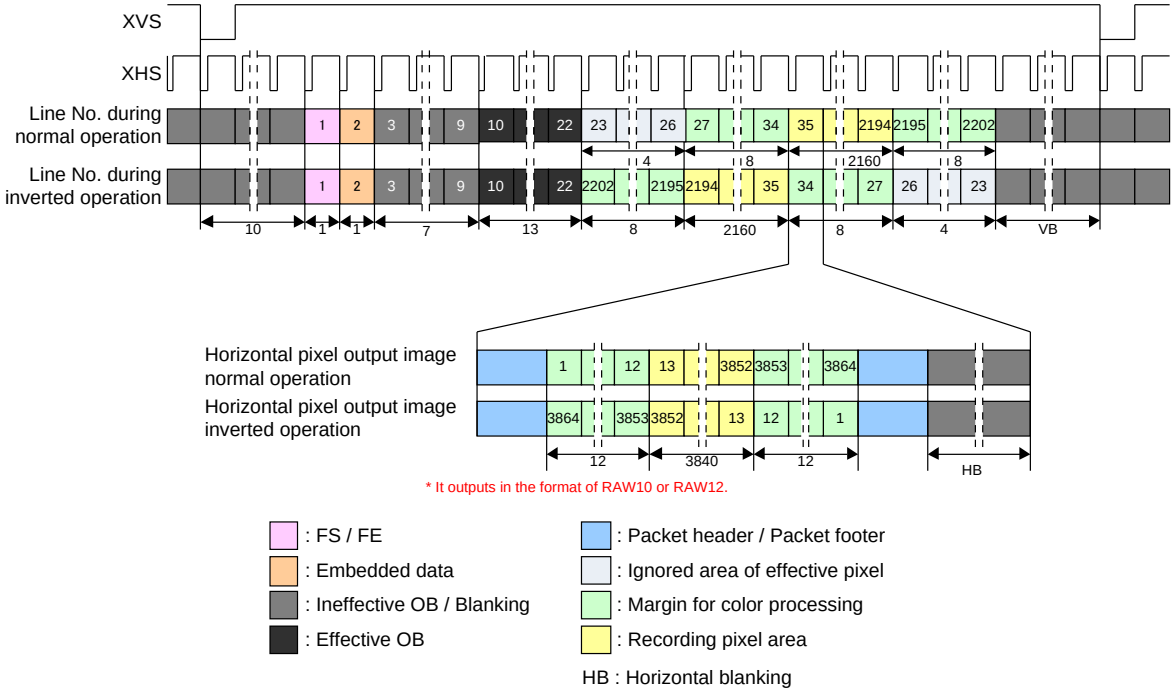
Address	bit	Register Name	Initial Value	CSI-2 serial								Remarks
				4 lane	8 lane	4lane	8lane	4 lane	8 lane	4lane	8lane	
				30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	60 / 50 [frame /s]	30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	60 / 50 [frame /s]	
AD Conversion [bit]				10	10	10	10	12	12	12	12	
Output bit width [bit]				10	10	10	10	12	12	12	12	
Data rate [Mbps/lane]				891/1188	891/1188	1782	891/1188	891/1188	891/1188	1782	891/1188	
3A18h	[7:0]	TCLKPOST	00B7h	007Fh /008Fh	007Fh /008Fh	00B7h	007Fh /008Fh	007Fh /008Fh	007Fh /008Fh	00B7h	007Fh /008Fh	Global timing 891Mbps/ 1188Mbps
3A19h	[7:0]											
3A1Ah	[7:0]	TCLKPREPARE	0067h	0037h /004Fh	0037h /004Fh	0067h	0037h /004Fh	0037h /004Fh	0037h /004Fh	0067h	0037h /004Fh	
3A1Bh	[7:0]											
3A1Ch	[7:0]	TCLKTRAIL	006Fh	0037h /0047h	0037h /0047h	006Fh	0037h /0047h	0037h /0047h	0037h /0047h	006Fh	0037h /0047h	
3A1Dh	[7:0]											
3A1Eh	[7:0]	TCLKZERO	01DFh	00F7h /0137h	00F7h /0137h	01DFh	00F7h /0137h	00F7h /0137h	00F7h /0137h	01DFh	00F7h /0137h	
3A1Fh	[7:0]											
3A20h	[7:0]	THSPREPARE	006Fh	003Fh /004Fh	003Fh /004Fh	006Fh	003Fh /004Fh	003Fh /004Fh	003Fh /004Fh	006Fh	003Fh /004Fh	
3A21h	[7:0]											
3A22h	[7:0]	THSZERO	00CFh	006Fh /0087h	006Fh /0087h	00CFh	006Fh /0087h	006Fh /0087h	006Fh /0087h	00CFh	006Fh /0087h	
3A23h	[7:0]											
3A24h	[7:0]	THSTRAIL	006Fh	003Fh /004Fh	003Fh /004Fh	006Fh	003Fh /004Fh	003Fh /004Fh	003Fh /004Fh	006Fh	003Fh /004Fh	
3A25h	[7:0]											
3A26h	[7:0]	THSEXIT	00B7h	005Fh /007Fh	005Fh /007Fh	00B7h	005Fh /007Fh	005Fh /007Fh	005Fh /007Fh	00B7h	005Fh /007Fh	
3A27h	[7:0]											
3A28h	[7:0]	TLPX	005Fh	002Fh /003Fh	002Fh /003Fh	005Fh	002Fh /003Fh	002Fh /003Fh	002Fh /003Fh	005Fh	002Fh /003Fh	
3A29h	[7:0]											

Set the following register depending on a read out mode.

Address	bit	Initial Value	Vertical readout direction	
			Normal	Inverted
3078h	[7:0]	02h	02h	02h
3079h	[7:0]	00h	00h	00h
307Ah	[7:0]	00h	00h	00h
307Bh	[7:0]	00h	00h	00h
3080h	[7:0]	02h	02h	FEh
3081h	[7:0]	00h	00h	00h
3082h	[7:0]	00h	00h	00h
3083h	[7:0]	00h	00h	00h
3088h	[7:0]	02h	02h	02h
3094h	[7:0]	00h	00h	00h
3095h	[7:0]	00h	00h	00h
3096h	[7:0]	00h	00h	00h
309Bh	[7:0]	02h	02h	FEh
309Ch	[7:0]	00h	00h	00h
309Dh	[7:0]	00h	00h	00h
309Eh	[7:0]	00h	00h	00h
30A4h	[7:0]	00h	00h	00h
30A5h	[7:0]	00h	00h	00h



Pixel Array Image Drawing in All scan mode



Drive Timing Chart for All scan mode

Horizontal/Vertical 2/2-line binning scan mode

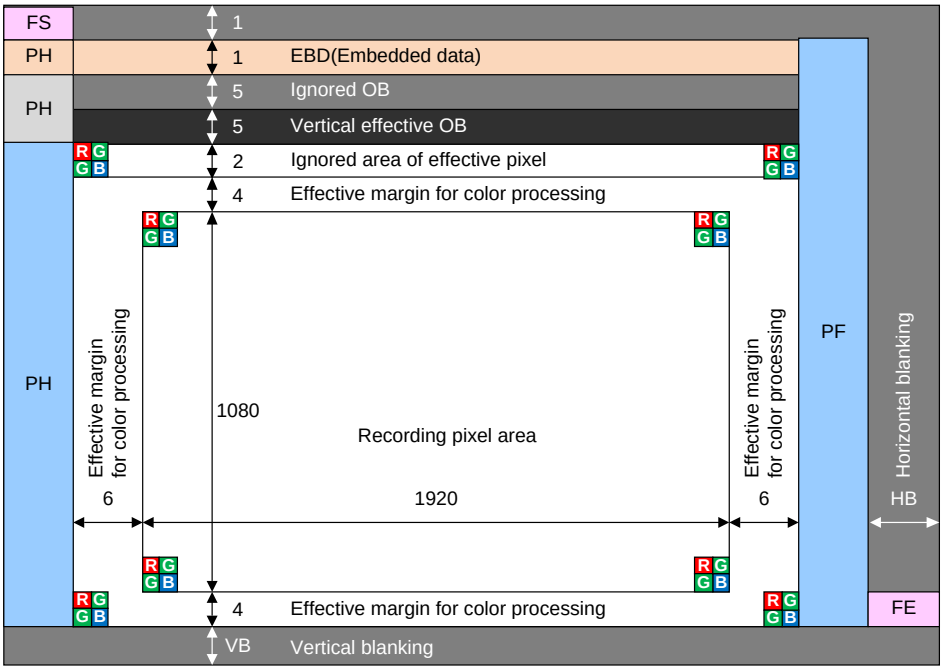
List of Setting Register

Address	bit	Register Name	Initial Value	CSI-2 serial					Remarks
				4 lane	8 lane	4lane	8lane	8 lane	
				30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	60 / 50 [frame /s]	120 [frame /s]	
AD Conversion [bit]				10	10	10	10	10	
Output bit width [bit]				12	12	12	12	12	
Data rate [Mbps/lane]				891/1188	891/1188	1188/1782	891/1188	1188	
3018h	[3:0]	WINMODE	0h	1h					
3030h	[7:0]	VMAX	08CAh	08CAh					25 /30 / 50 / 60 [frame/s]
3031h	[7:0]								
3032h	[3:0]								
3034h	[7:0]	HMAX	0226h	044Ch / 0528h	044Ch / 0528h	0226h / 0294h	0226h / 0294h	0113h	30 / 25[frame / s] / 60 / 50[frame / s]
3035h	[7:0]								
304Ch	[7:0]	OPB_SIZE_V	014h	14h					
304Eh	[7:0]	HREVERSE	00h	00h / 01h					0: Normal , 1: Inverted
304Fh	[7:0]	VREVERSE	00h	00h / 01h					0: Normal, 1: Inverted
3050h	[7:0]	ADBIT	01h	00h					0: 10 bit
3074h	[7:0]	AREA3_ST_ ADR_1	00B0h	Normal：00B0h Inverted：11C0h					
3075h	[4:0]								
308Eh	[7:0]	AREA3_ST_ ADR_2	00B1h	Normal：00B1h Inverted：11C1h					
308Fh	[4:0]								
30B6h	[7:0]	UNREAD_ PARAM5	00h	Normal：0000h Inverted：01FAh					
30B7h	[0]								
3114h	[7:0]	UNREAD_ PARAM6	08h	Normal：0008h Inverted：0002h					
3115h	[0]								
314Ch	[7:0]	INCKSEL1	00C0h	Refer to “INCK setting”					
314Dh	[0]								
315Ah	[1:0]	INCKSEL2	3h						
	[3:2]	PLL_IF_GC	0h						
3168h	[7:0]	INCKSEL3	68h						
316Ah	[1:0]	INCKSEL4	3h						
3199h	[4]	HADD	0h	3h					
	[5]	VADD							
319Dh	[0]	MDBIT	1h	1h					
319Eh	[1:0]	SYS_MODE	0h	Refer to “INCK setting”					
31DDh	[2:0]	VALID_EXPAND	3h	4h					
3300h	[1:0]	TCYCLE	0h	1h					
3308h	[7:0]	Y_OUT_SIZE	0884h	0442h					
3309h	[4:0]								
341Ch	[7:0]	ADBIT1	0047h	01FFh					
341Dh	[0]								
3A01h	[2:0]	LANEMODE	3h	3h	7h	3h	7h	7h	

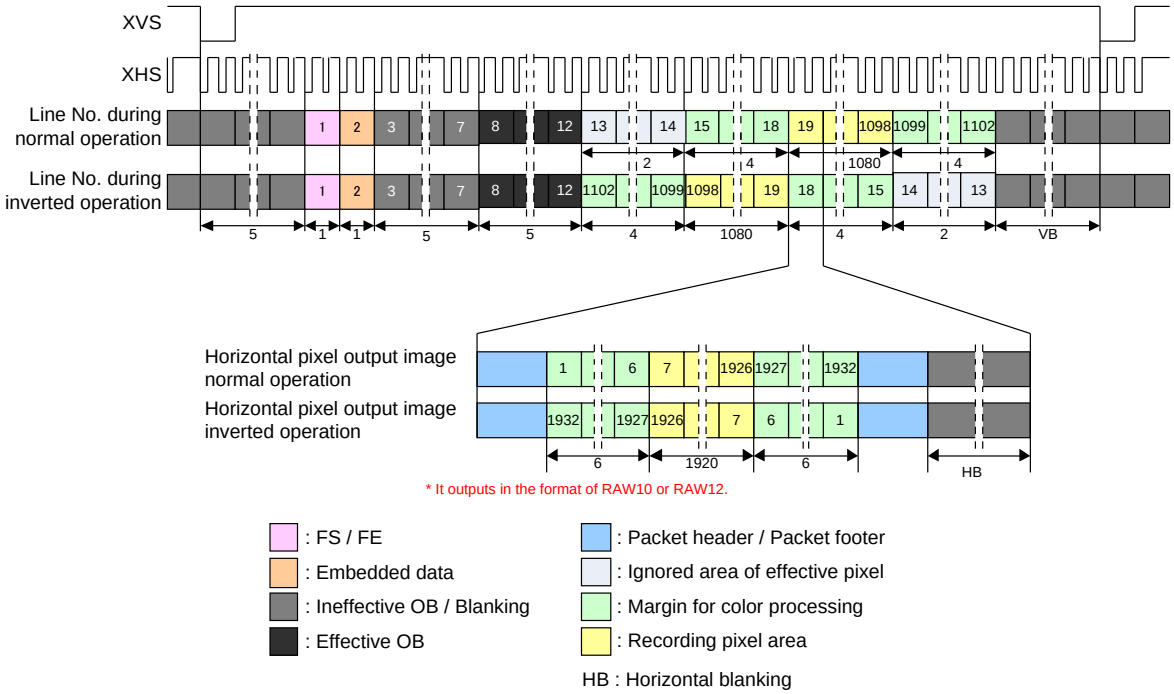
Address	bit	Register Name	Initial Value	CSI-2 serial					Remarks
				4 lane	8 lane	4lane	8lane	8 lane	
				30 / 25 [frame /s]	30 / 25 [frame /s]	60 / 50 [frame /s]	60 / 50 [frame /s]	120 [frame /s]	
AD Conversion [bit]				10	10	10	10	10	
Output bit width [bit]				12	12	12	12	12	
Data rate [Mbps/lane]				891/1188	891/1188	1188/1782	891/1188	1188	
3A18h	[7:0]	TCLKPOST	00B7h	007Fh /008Fh	007Fh /008Fh	008Fh /00B7h	007Fh /008Fh	008Fh	Global timing 891Mbps/ 1188Mbps 1188Mbps/ 1782Mbps
3A19h	[7:0]								
3A1Ah	[7:0]	TCLKPREPARE	0067h	0037h /004Fh	0037h /004Fh	004Fh /0067h	0037h /004Fh	004Fh	
3A1Bh	[7:0]								
3A1Ch	[7:0]	TCLKTRAIL	006Fh	0037h /0047h	0037h /0047h	0047h /006Fh	0037h /0047h	0047h	
3A1Dh	[7:0]								
3A1Eh	[7:0]	TCLKZERO	01DFh	00F7h /0137h	00F7h /0137h	0137h/ 01DFh	00F7h /0137h	0137h	
3A1Fh	[7:0]								
3A20h	[7:0]	THSPREPARE	006Fh	003Fh /004Fh	003Fh /004Fh	004Fh /006Fh	003Fh /004Fh	004Fh	
3A21h	[7:0]								
3A22h	[7:0]	THSZERO	00CFh	006Fh /0087h	006Fh /0087h	0087h /00CFh	006Fh /0087h	0087h	
3A23h	[7:0]								
3A24h	[7:0]	THSTRAIL	006Fh	003Fh /004Fh	003Fh /004Fh	004Fh /006Fh	003Fh /004Fh	004Fh	
3A25h	[7:0]								
3A26h	[7:0]	THSEXIT	00B7h	005Fh /007Fh	005Fh /007Fh	007Fh /00B7h	005Fh /007Fh	007Fh	
3A27h	[7:0]								
3A28h	[7:0]	TLPX	005Fh	002Fh /003Fh	002Fh /003Fh	003Fh /005Fh	002Fh /003Fh	003Fh	
3A29h	[7:0]								

Set the following register depending on a read out mode.

Address	bit	Initial Value	Vertical readout direction	
			Normal	Inverted
3078h	[7:0]	02h	04h	04h
3079h	[7:0]	00h	FEh	FEh
307Ah	[7:0]	00h	04h	04h
307Bh	[7:0]	00h	02h	02h
3080h	[7:0]	02h	04h	FCh
3081h	[7:0]	00h	FEh	02h
3082h	[7:0]	00h	04h	FCh
3083h	[7:0]	00h	02h	FEh
3088h	[7:0]	02h	04h	04h
3094h	[7:0]	00h	FEh	FEh
3095h	[7:0]	00h	04h	04h
3096h	[7:0]	00h	02h	02h
309Bh	[7:0]	02h	04h	FCh
309Ch	[7:0]	00h	FEh	02h
309Dh	[7:0]	00h	04h	FCh
309Eh	[7:0]	00h	02h	FEh
30A4h	[7:0]	00h	33h	33h
30A5h	[7:0]	00h	33h	33h



Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binnign scan mode



Drive Timing Chart for Horizontal /Vertical 2/2-line binnign scan mode

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
Cropping position is set, regarding effective pixel start position as origin (48, 176) in normal mode or (48, 4544) in inverted direction all pixel scan mode. The horizontal normal or inverted operation don't relate to the origin.

Cropping is available from all-pixel scan mode and vertical, horizontal period and frame rate are fixed to the value for this mode. Pixels cropped by horizontal cropping setting are output with left shifted and that extends the horizontal blanking period.
Window cropping image is shown in the figure below.
This function support only All-pixel scan mode.

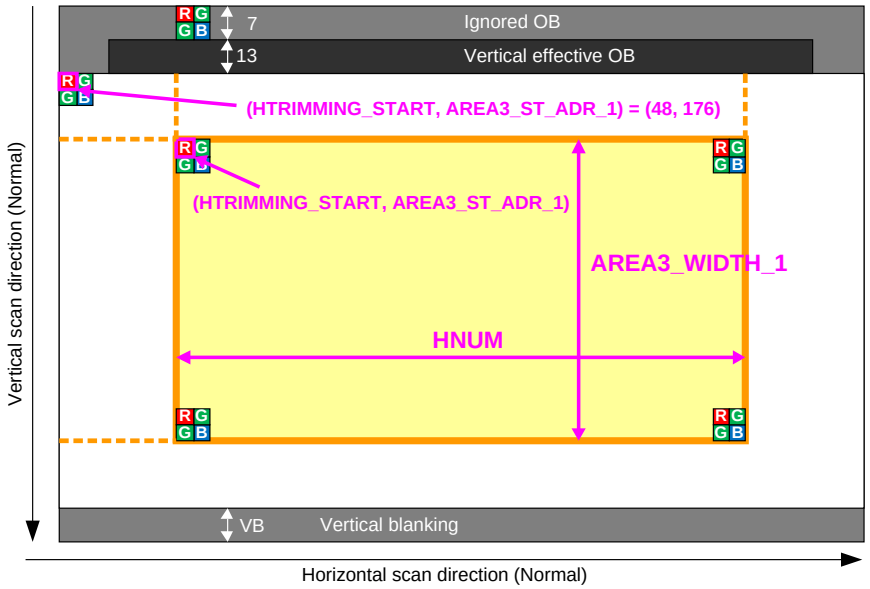


Image Drawing of Window Cropping Mode in normal vertical direction

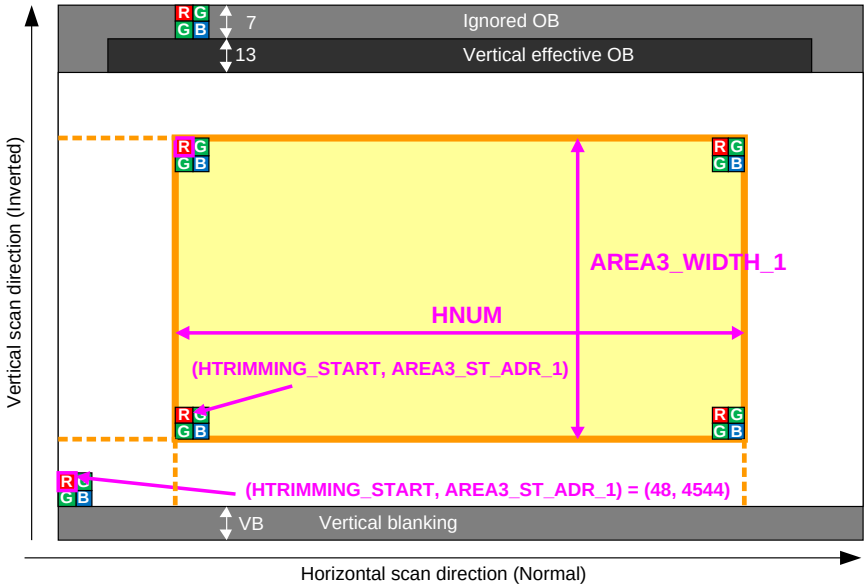


Image Drawing of Window Cropping Mode in inverted vertical direction

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

Set WINMODE: 4h.

◆ HTRIMMING_START, HNUM

48 ≤ HTRIMMING_START + HNUM ≤ 3912
HTRIMMING_START = 48 + N×12
312 ≤ HNUM
Set HNUM to a multiple of 24.
(N is integer equal or more than 0)

◆ AREA3_ST_ADR_1, AREA3_ST_ADR_2

In case of VREVERSE = 00h
AREA3_ST_ADR_1 = 176 + M×4
AREA3_ST_ADR_2 = AREA3_ST_ADR_1 + 1
M is integer equal or more than 0.
It sets a half value of the number of the skipping lines in M.

In case of VREVERSE = 01h
AREA3_ST_ADR_1 = 4544 - M×4
AREA3_ST_ADR_2 = AREA3_ST_ADR_1 + 1
M is integer equal or more than 0.
It sets a half value of the number of the skipping lines in M.

◆ AREA3_WIDTH_1, AREA3_WIDTH_2, Y_OUT_SIZE

372 ≤ AREA3_WIDTH_1 ≤ 2180
Set AREA3_WIDTH_1 to multiple of 2.
AREA3_WIDTH_2 = AREA3_WIDTH_1
Set Y_OUT_SIZE to same as AREA3_WIDTH_1.

◆ UNREAD_ED_ADR

UNREAD_ED_ADR = AREA3_ST_ADR_1 + AREA3_WIDTH_1×2 + 208
In case of UNREAD_ED_ADR ＞ 4640 , set UNREAD_ED_ADR = 4640

◆ UNRD_LINE_MAX, BLACK_OFSET_ADR

In case of VREVERSE = 00h and 176 ≤ AREA3_ST_ADR_1 ＜276
or VREVERSE = 01h and 4444＜AREA3_ST_ADR_1 ≤ 4544
set UNRD_LINE_MAX = 0
BLACK_OFSET_ADR = 0

In case of VREVERSE = 00h and 276 ≤ AREA3_ST_ADR_1
or VREVERSE = 01h and AREA3_ST_ADR_1 ≤ 4444
set UNRD_LINE_MAX = 100
BLACK_OFSET_ADR = 18

V_{TTL} (1frame line length or VMAX) ≥ AREA3_WIDTH_1 + 48

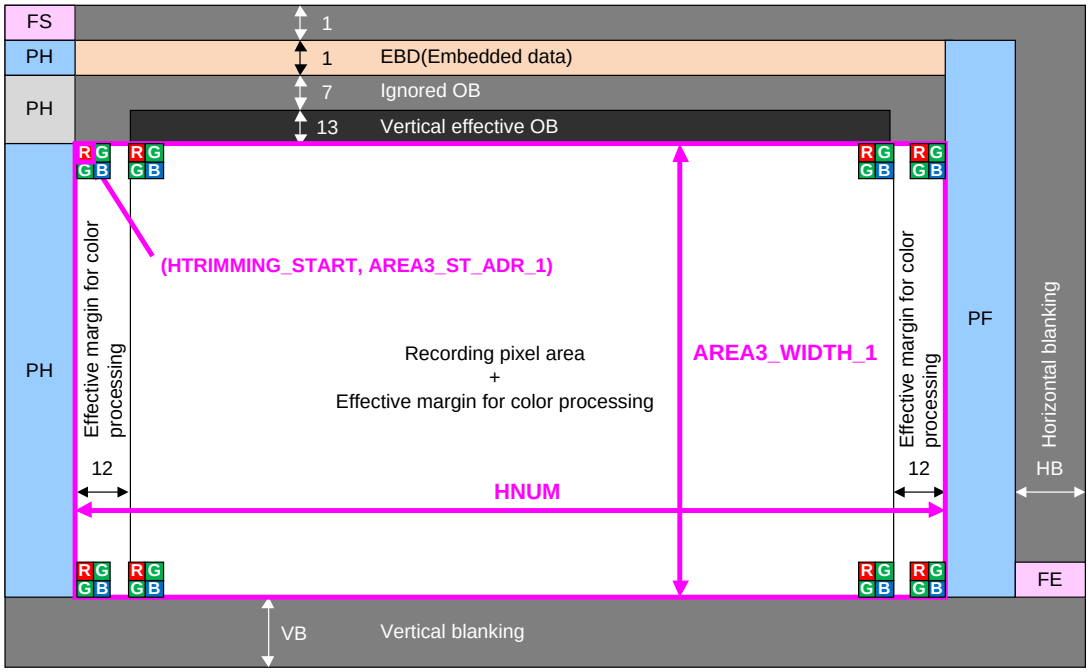
◆ Frame rate on Window cropping mode

Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))
1H period (unit: [μs]) : Fix 1H time in a mode before cropping and refer to the value of "1H period" in the table of "Operating Mode".

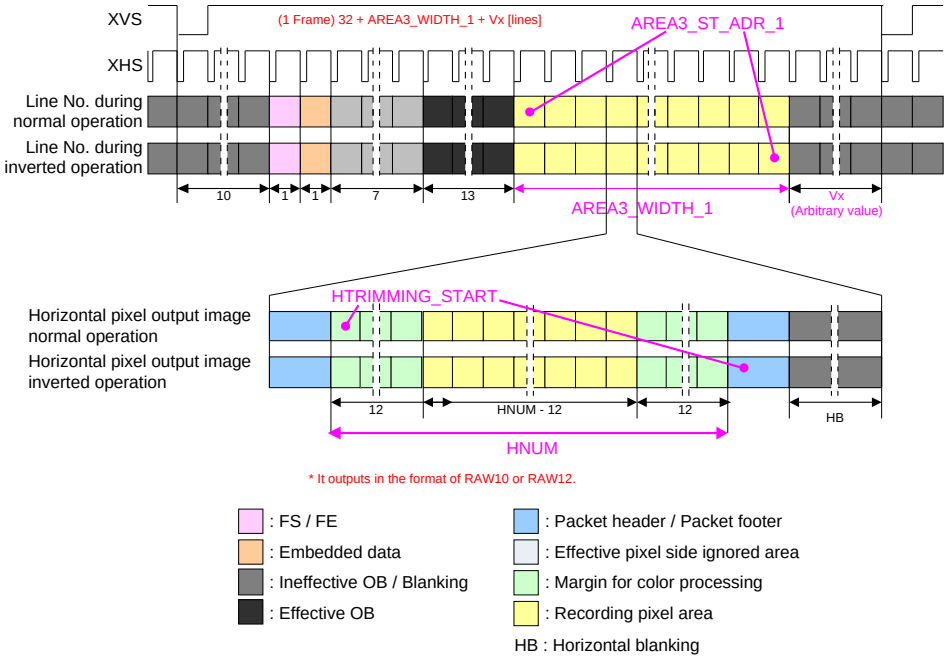
The example of window cropping setting is shown below.
The frame rate is maximum setting as each image format. For adjusting the frame rate, please extend the VMAX or the number of lines per frame.

Example of Window cropping Mode Setting

Number of active pixels				1944×1100	
Recording Pixels				1920×1080	
Lane number				4lane	
Frame rate [frame/s]				117	117
AD Conversion [bit]				10	12
Output bit width [bit]				10	12
Data rate [Mbps/lane]				1782	1782
Address	bit	Register Name	Initial Value	Register Setting	
3018h	[3:0]	WINMODE	0h	4h	4h
3030h	[7:0]	VMAX	08CAh	047Ch	047Ch
3031h	[7:0]				
3032h	[3:0]				
3034h	[7:0]	HMAX	0226h	0226h	0226h
3035h	[7:0]				
302Ch	[7:0]	HTRIMMING_START	0030h	03F0h	03F0h
302Dh	[7:0]				
302Eh	[7:0]	HNUM	0F18h	0798h	0798h
302Fh	[7:0]				
3074h	[7:0]	AREA3_ST_ADR_1	0000h	04E8h	04E8h
3075h	[4:0]				
3076h	[7:0]	AREA3_WIDTH_1	0884h	044Ch	044Ch
3077h	[4:0]				
308Eh	[7:0]	AREA3_ST_ADR_2	0001h	04E9h	04E9h
308Fh	[4:0]				
3090h	[7:0]	AREA3_WIDTH_2	0884h	044Ch	044Ch
3091h	[4:0]				
30C6h	[7:0]	BLACK_OFSET_ADR	0000h	0012h	0012h
30C7h	[4:0]				
30CEh	[7:0]	UNRD_LINE_MAX	0000h	0064h	0064h
30CFh	[4:0]				
30D8h	[7:0]	UNREAD_ED_ADR	118Fh	0E50h	0E50h
30D9h	[3:0]				
3308h	[7:0]	Y_OUT_SIZE	0884h	044Ch	044Ch
3309h	[4:0]				



Pixel Array Image Drawing in Window Cropping mode (CSI-2 serial output)



Drive Timing Chart for Window Cropping mode (CSI-2 serial output)

Description of Various Function

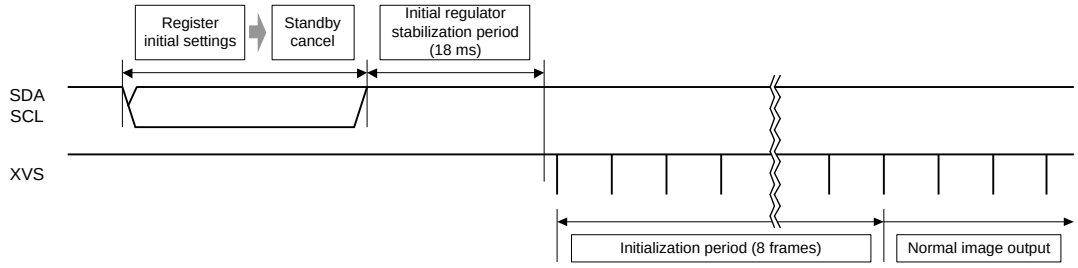
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register name	Register details			Initial value	Setting value	Status	Remarks
	Register	Address	bit				
STANDBY	—	3000h	[0]	1	1	Standby	Register communication is executed in standby mode.
					0	Operating	

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to “0”. Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the 9 frames after internal regulator stabilization (18 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)

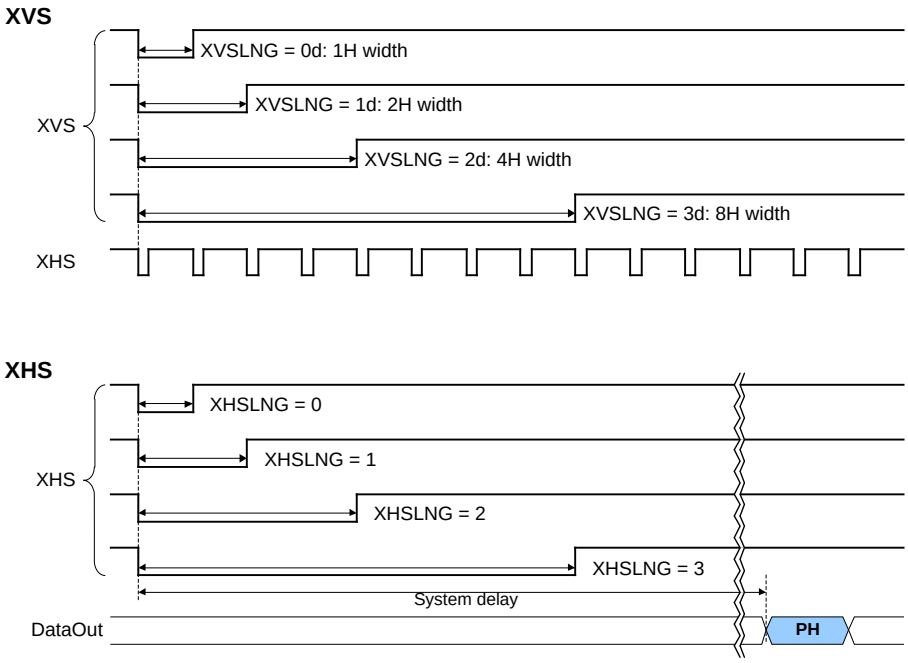
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Operating mode" for the number of output data line and 1H period.
Set the XVSOUTSE, XHSOUTSEL, XVS_DRV, XHS_DRV and XMSTA register in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [19:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of Operation Mode for details of the section of “Operating Modes”.

List of Slave and Master Mode Setting

Pin name	Pin processing	Operating mode	Remarks
XMASTER pin	Fixed to Low	Master mode	High: OV_{DD}
	Fixed to High	Slave mode	Low: GND

List of Register in Master Mode

Register name	Register details			Initial value	Setting value	Remarks
	Register	Address	bit			
XMSTA	—	3002h	[0]	1h	1: Master operation ready 0: Master operation start	The master operation starts by setting 0.
VMAX [19:0]	VMAX [7:0]	3030h	[7:0]	008CAh	See the item of each drive mode.	Line number per frame designated
	VMAX [15:8]	3031h	[7:0]			
	VMAX [19:16]	3032h	[4:0]			
HMAX [15:0]	HMAX [7:0]	3034h	[7:0]	0226h	See the item of each drive mode.	Clock number per line designated
	HMAX [15:8]	3035h	[7:0]			
XVSLNG [1:0]	—	31D4h	[5:4]	0h	0: 1H, 1: 2H, 2: 4H, 3: 8H	XVS low level pulse width designated
XHSLNG [1:0]	—	31D5h	[5:4]	0h	0: 16clock, 1: 32clock 2: 64clock, 3: 128clock See the next	XHS low level pulse width designated
XVSOUTSEL [1:0]	—	31A0h	[1:0]	2h	0: Fixed to Low 2: VSYNC output Others: Setting prohibited	
XHSOUTSEL [1:0]	—		[3:2]	2h	0: Fixed to Low 2: HSYNC output Others: Setting prohibited	
XVS_DRV [1:0]	—	31A1h	[1:0]	3h	0: XVS output (Master mode) 3: Hi-z (Slave mode) Others: Setting prohibited	
XHS_DRV [1:0]	—		[3:2]	3h	0: XHS output (Master mode) 3: Hi-z (Slave mode) Others: Setting prohibited	



XVS/XHS output waveform in sensor master mode

The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output Kust after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with a undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to 72.0dB by the GAIN [7:0] register setting. The same setting is applied in all colors.

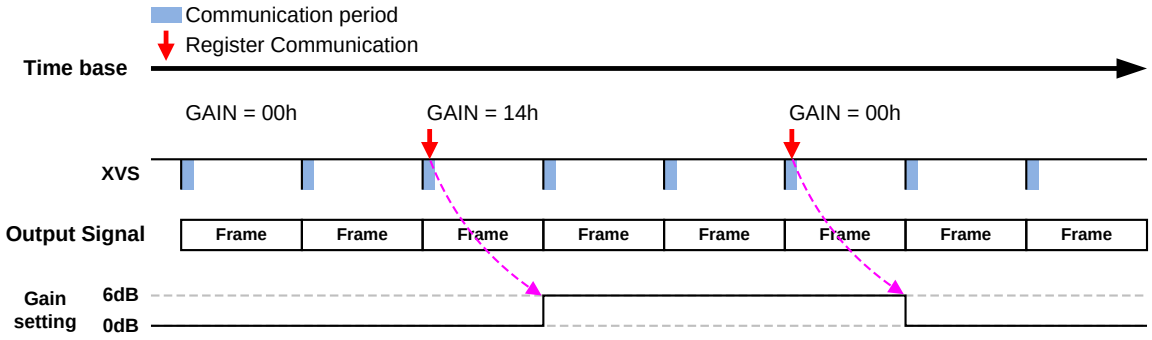
The value which is 10/3 times the gain is set to register. (0.3 dB step)

Example)
When set to 6 dB: 6 × 10/3 = 20d; GAIN [7:0] = 14h
When set to 12.6 dB: 12.6 × 10/3 = 42d; GAIN [7:0] = 2Ah

List of PGC Register

Register name	Register details			Initial value	Setting value	Remarks
	Register	Address	bit		Setting range	
GAIN [10:0]	GAIN [7:0]	30E8h	[7:0]	00h	00h-F0h (0d-240d)	Setting value: Gain [dB] × 10/3 (0.3 dB step)
	GAIN [10:8]	30E9h	[2:0]	00h		

The gain setting is reflected at the next frame that the communication is performed as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 3FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [9:0] register.
When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB at 10.
Note that the offset unit changes according to the output bit setting.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 LSB. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 LSB.

Use with values shown below is recommended.
10-bit output: 032h (50d)
12-bit output: 032h (200d)

List of Black Level AdKustment Register

Register name	Register details			Initial value	Setting value
	Register	Address	bit		
BLKLEVEL [9:0]	BLKLEVEL [7:0]	3302h	[7:0]	032h	000h to 3FFh
	BLKLEVEL [9:8]	3303h	[1:0]		

Normal Operation and Inverted Operation

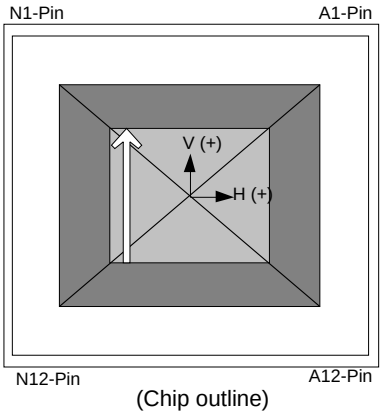
The sensor readout direction (normal / inverted) in vertical direction can be switched by VREVERSE register settings and in horizontal direction can be switched by the HREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. See the section of “List of Setting Register” for the other register settings. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Drive Direction Setting Register

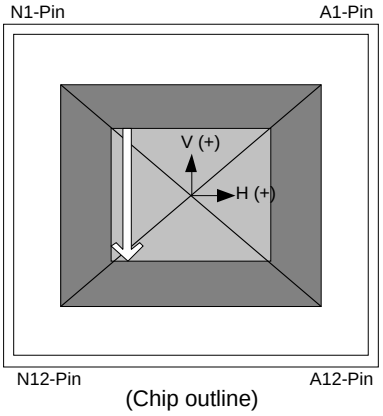
Vertical direction normal and inverted modes

Address	bit	Register name	Initial value	Normal	Inverted
304Fh	[0]	VREVERSE	00h	00h	01h
304Eh	[0]	HREVERSE	00h	00h	01h

In normal mode

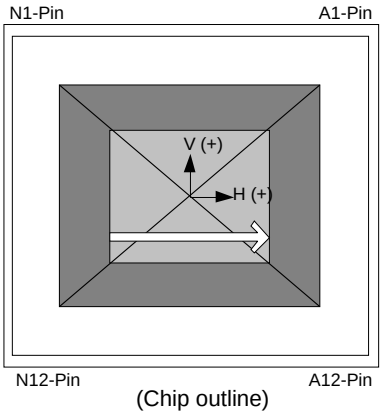


In inverted mode

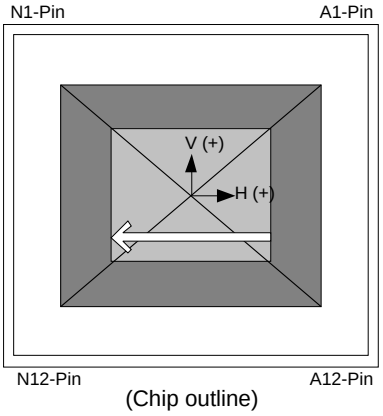


Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)

In normal mode



In inverted mode



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - SHR0 × (1H period)

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
*2 See “Operating Modes” for the 1H period.

In this section, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

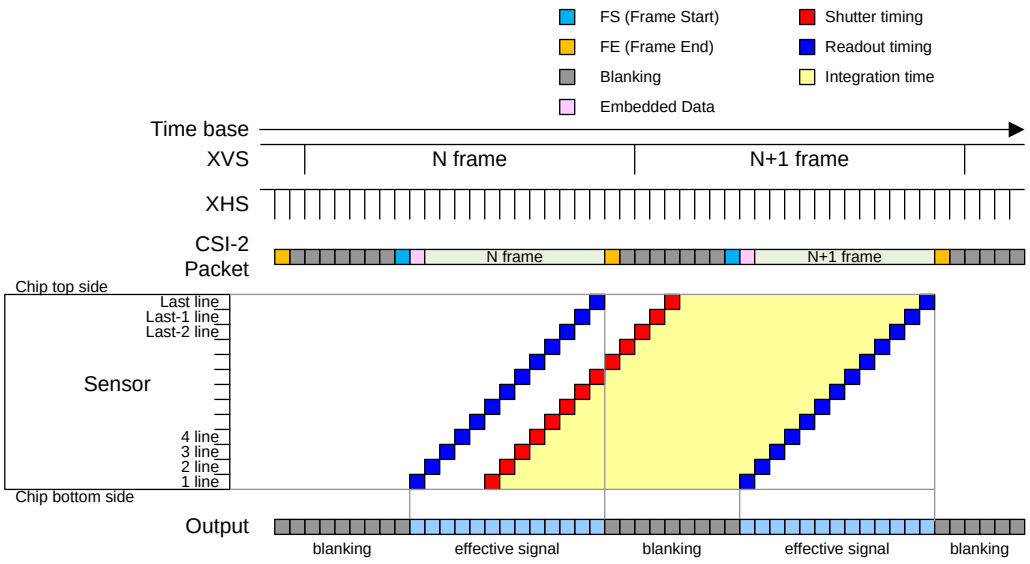


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHR0 [19:0] register. Set SHR0 [19:0] to a value between 5 and (Number of lines per frame - 1). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register. The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 1H Units

Register name	Register details			Initial value	Setting value
	Register	Address	bit		
SHR0 [19:0]	SHR0 [7:0]	3058h	[7:0]	00005h	Sets the shutter sweep time. 5 to (Number of lines per frame - 1) * Others: Setting prohibited
	SHR0 [15:8]	3059h	[7:0]		
	SHR0 [19:16]	305Ah	[3:0]		
VMAX [19:0]	VMAX [7:0]	3030h	[7:0]	008CAh	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	VMAX [15:8]	3031h	[7:0]		
	VMAX [19:16]	3032h	[3:0]		

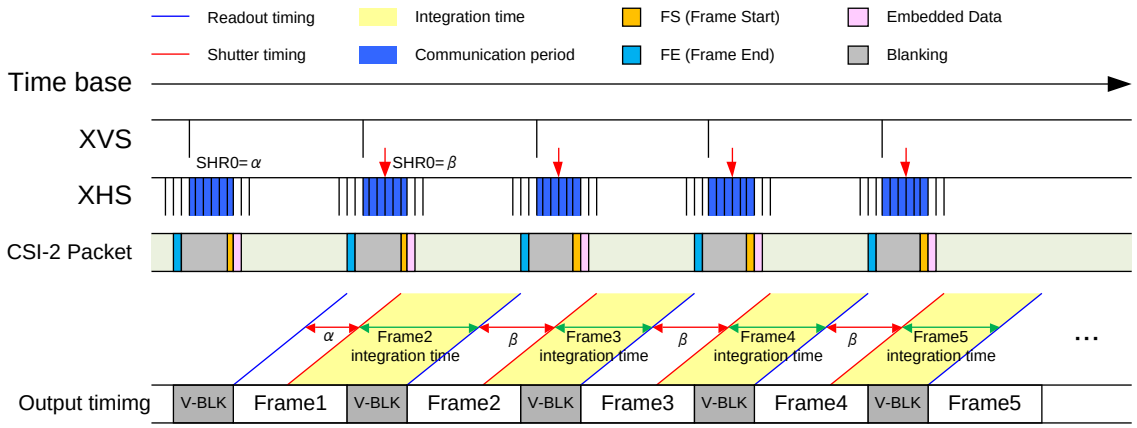


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [19:0] value compared to normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

Although the maximum value of long exposure operation changes in each modes, the maximum of long time exposure is approximately 1 s.
When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

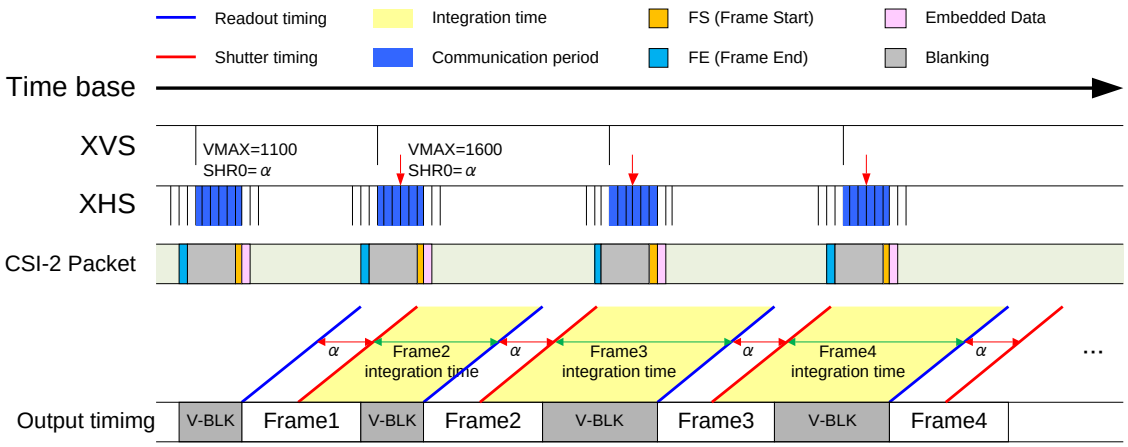


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Settings

Operation	Sensor setting (register)		Integration time
	VMAX*	SHR0**	
All-pixel scan mode	2250	2249	1H
		⋮	⋮
		N	(2250 - N) H
		⋮	⋮
		5	2245H

* In sensor master mode. In slave mode, the interval is the same as XVS input.
** The SHR0 setting value (N) is set between “5” and “the VMAX value (M) – 1”.

Signal Output
CSI-2 output

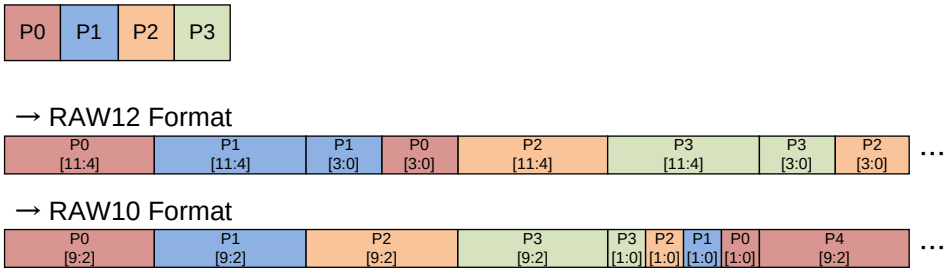
The output formats of this sensor support the following modes.

CSI-2 serial 4 Lane / 8 Lane, RAW10 / RAW12

The 4 Lane / 8 Lane serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 4 Lane / 8 Lane. The image data is output from the CSI-2 output pin. The DMOP1/DMOM1 are called the Lane1 data signal, the DMOP2/DMOM2 are called the Lane2 data signal, the DMOP3/DMOM3 are called the Lane3 data signal, the DMOP4/DMOM4 are called the Lane4 data signal, the DMOP5/DMOM5 are called the Lane5 data signal, the DMOP6/DMOM6 are called the Lane6, the DMOP7/DMOM7 are called the Lane7 data signal data signal, the DMOP8/DMOM8 are called the Lane8 data signal. In addition, the clock signals are output from DMCKP/DMCKM of the CSI-2 pins.
In 4 Lane mode, data is output from Lane1 , Lane2 , Lane3 and Lane4. In 8 Lane mode, data is output from Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7 and Lane8. The bit rate maximum value are 1782 Mbps / Lane in 4 Lane mode and 1188 Mbps / Lane in 8 Lane mode..
The select of RAW10 / RAW12 is set by the register: MDBIT [0]. The number of output lanes is set by the register: LANEMODE [2:0]. Unused lanes (when setting4 lanes; DMOP5 / DMOM5, DMOP6 / DMOM6, DMOP7 / DMOM7, DMOP8 / DMOM8) output signals conformed to MIPI standard.

Register name	Register details		Initial value	Setting value	Description
	Address	bit			
MDBIT	319Dh	[0]	1h	0h	RAW10
				1h	RAW12
LANEMODE [2:0]	3A01h	[2:0]	3h	3h	4Lane
				7h	8Lane
				-	Others:Setting prohibited

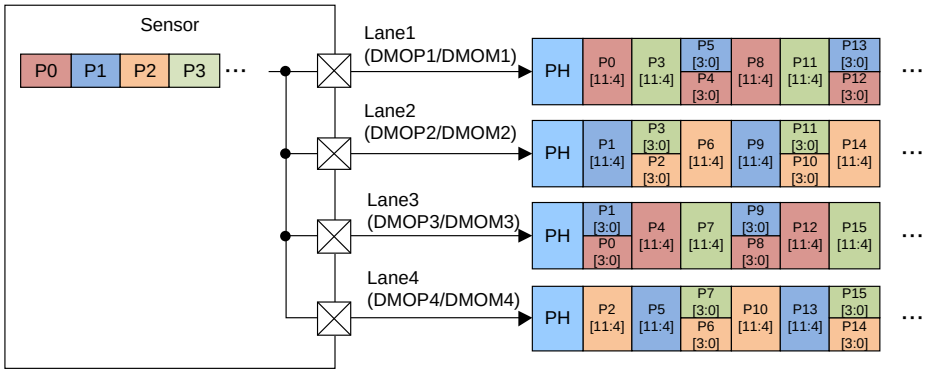
The formats of RAW12 and RAW10 are shown below.



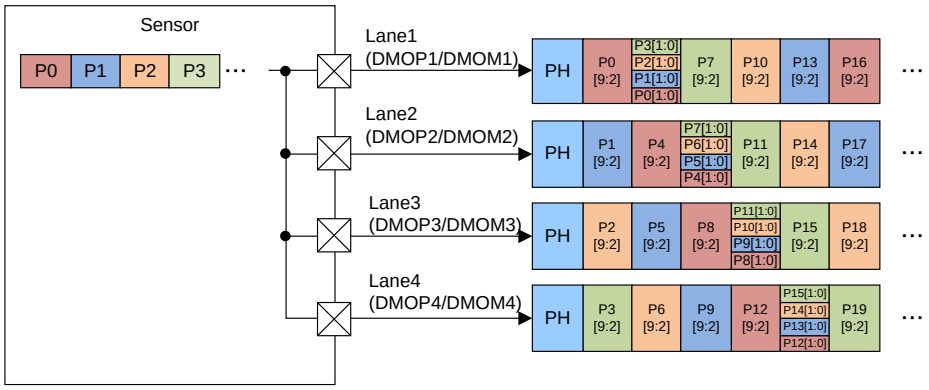
The Example of Format of RAW12 / RAW10

The each formal of 4 Lane and 8 Lane are shown below.

a) 4 Lane-RAW12

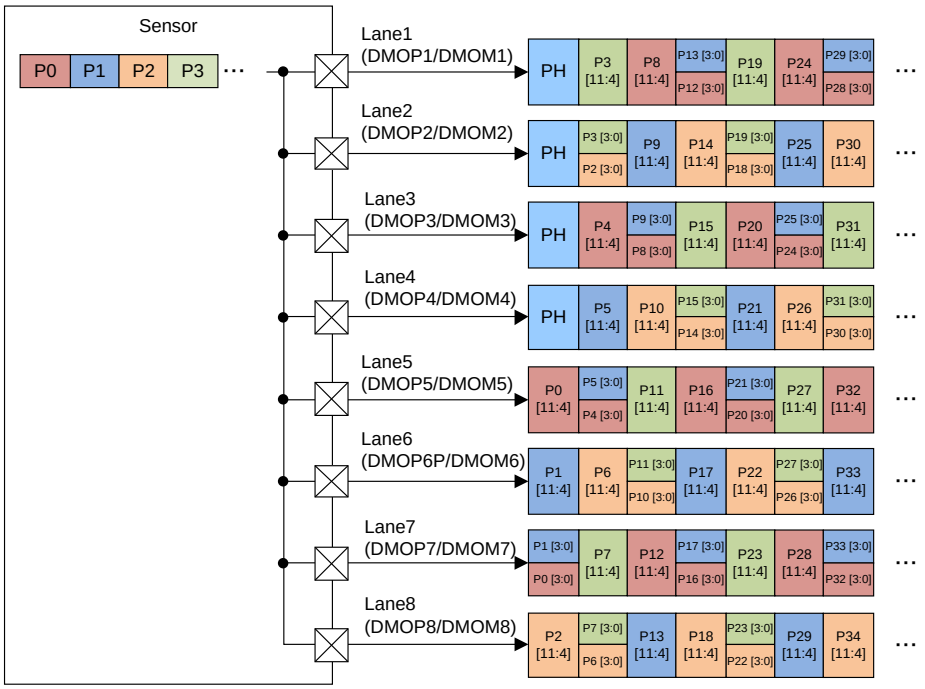


b) 4 Lane-RAW10

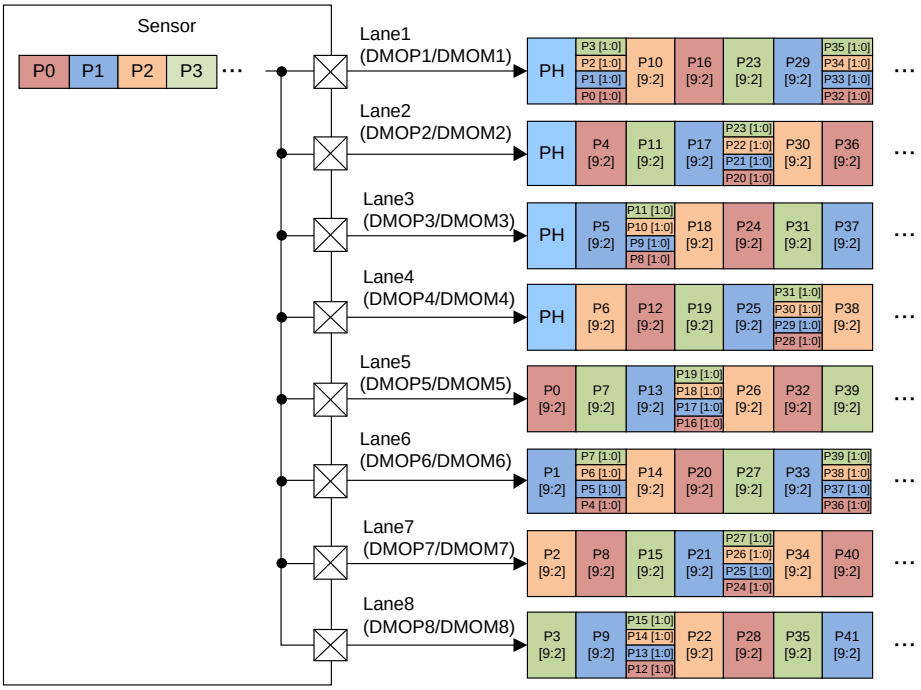


4 Lane Output Format

c) 8 Lane-RAW12



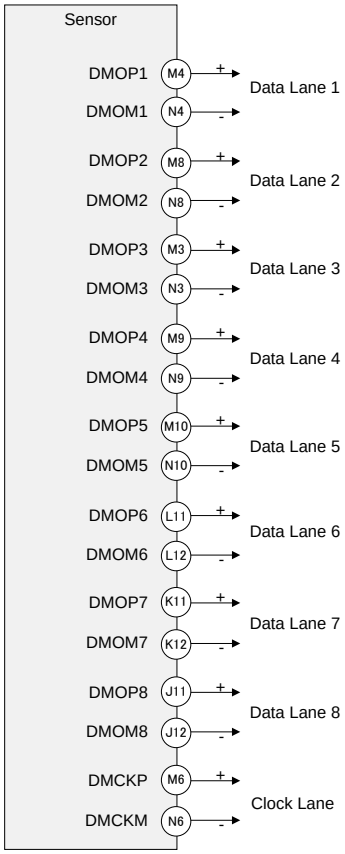
d) 8 Lane-RAW10



8 Lane Output Format

MIPI Transmitter

Output pins (DMOP1, DMOM1, DMOP2, DMOM2, DMOP3, DMOM3, DMOP4, DMOM4, DMOP5, DMOM5, DMOP6, DMOM6, DMOP7, DMOM7, DMOP8, DMOM8, DMCKP, DMCKM) are described in this section.

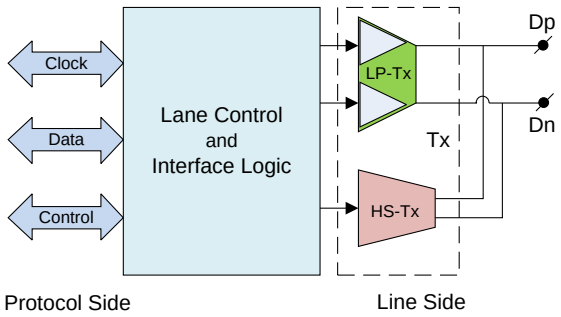


Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard

- MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.20.00
- MIPI Alliance Specification for D-PHY Version 1.20.00

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 1782 Mbps / Lane.



Universal Lane Module Functions

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bits or 12 bits by the register ADBIT. See the section of “Operating Modes” for the correspondence with each mode.

List of Bit Width Selection

Register name	Register details			Initial value	Setting value
	Register	Address	bit		
ADBIT	—	3050h	[0]	1h	0: 10 bit 1: 12 bit
ADBIT1[8:0]	ADBIT1[7:0]	341Ch	[7:0]	0047h	10 bit: 01FFh 12 bit: 0047h
	ADBIT1[8]	341Dh	[0]		

Output Signal Range

In CSI-2 output mode, the sensor output has either a 10 bit or 12 bit gradation, but output is not performed over the full range, and the maximum output value is the 3FFh value (10 bit output) and the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh
12 bit	000h	FFFh

INCK Setting

The available operation mode varies according to INCK frequency. Input either 6-27 MHz ,37.125 MHz or 74.25 MHz for INCK frequency. The INCK setting register and the list of INCK setting are shown in the table below.

INCK Setting Register

Data rate 1782Mbps / lane

Register name	Register details			Initial value	INCK						
	Register	Address	bit		6 [MHz]	12 [MHz]	18 [MHz]	24 [MHz]	27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	—	300Ch	[7:0]	B6h	0Fh	1Eh	2Dh	3Bh	42h	5Bh	B6h
CPWAIT_TIME	—	300Dh	[7:0]	7Fh	0Bh	15h	1Fh	2Ah	2Eh	40h	7Fh
INCKSEL1	—	314D-4Ch	[8:0]	00C0h	0129h	0129h	00C6h	0129h	0108h	00C0h	00C0h
INCKSEL2	—	315Ah	[1:0]	3h	0h	1h	1h	2h	2h	2h	3h
PLL_IF_GC	—		[3:2]	0h	0h	0h	0h	0h	0h	0h	0h
INCKSEL3	—	3168h	[7:0]	68h	A0h	A0h	6Bh	A0h	8Fh	68h	68h
INCKSEL4	—	316Ah	[7:0]	7Fh	7Ch	7Dh	7Dh	7Eh	7Eh	7Eh	7Fh
SYS_MODE	—	319Eh	[7:0]	00h	00h	00h	00h	00h	00h	00h	00h

Data rate 1188Mbps / lane

Register name	Register details			Initial value	INCK						
	Register	Address	bit		6 [MHz]	12 [MHz]	18 [MHz]	24 [MHz]	27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	—	300Ch	[7:0]	B6h	0Fh	1Eh	2Dh	3Bh	42h	5Bh	B6h
CPWAIT_TIME	—	300Dh	[7:0]	7Fh	0Bh	15h	1Fh	2Ah	2Eh	40h	7Fh
INCKSEL1	—	314D-4Ch	[8:0]	00C0h	00C6h	00C6h	0084h	00C6h	00B0h	0080h	0080h
INCKSEL2	—	315Ah	[1:0]	3h	0h	1h	1h	2h	2h	2h	3h
PLL_IF_GC	—		[3:2]	0h	0h	0h	0h	0h	0h	0h	0h
INCKSEL3	—	3168h	[7:0]	68h	A0h	A0h	6Bh	A0h	8Fh	68h	68h
INCKSEL4	—	316Ah	[7:0]	7Fh	7Ch	7Dh	7Dh	7Eh	7Eh	7Eh	7Fh
SYS_MODE	—	319Eh	[7:0]	00h	01h	01h	01h	01h	01h	01h	01h

Data rate 891Mbps / lane

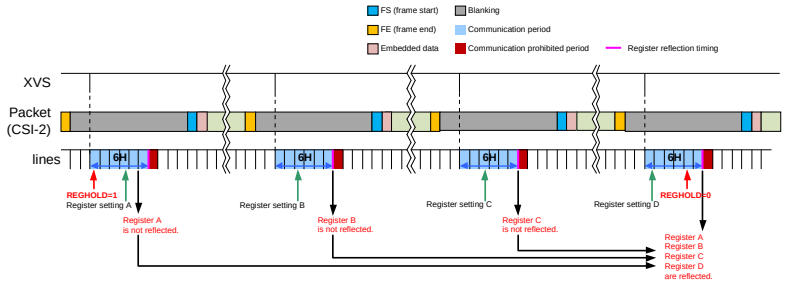
Register name	Register details			Initial value	INCK						
	Register	Address	bit		6 [MHz]	12 [MHz]	18 [MHz]	24 [MHz]	27 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	—	300Ch	[7:0]	B6h	0Fh	1Eh	2Dh	3Bh	42h	5Bh	B6h
CPWAIT_TIME	—	300Dh	[7:0]	7Fh	0Bh	15h	1Fh	2Ah	2Eh	40h	7Fh
INCKSEL1	—	314D-4Ch	[8:0]	00C0h	0129h	0129h	00C6h	0129h	0108h	00C0h	00C0h
INCKSEL2	—	315Ah	[1:0]	3h	0h	1h	1h	2h	2h	2h	3h
PLL_IF_GC	—		[3:2]	0h	1h	1h	1h	1h	1h	1h	1h
INCKSEL3	—	3168h	[7:0]	68h	A0h	A0h	6Bh	A0h	8Fh	68h	68h
INCKSEL4	—	316Ah	[7:0]	7Fh	7Ch	7Dh	7Dh	7Eh	7Eh	7Eh	7Fh
SYS_MODE	—	319Eh	[7:0]	00h	02h	02h	02h	02h	02h	02h	02h

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register Hold Setting Register

Register name	Register details			Initial value	Setting value
	Register	Address	bit		
REGHOLD	—	3001h	[0]	0h	0: Invalid 1: Valid (Register hold)



Register Hold Setting

Mode Transitions

When changing the operating mode during sensor drive operation, set via sensor standby. However, these transitions that described below can be transitions without standby.

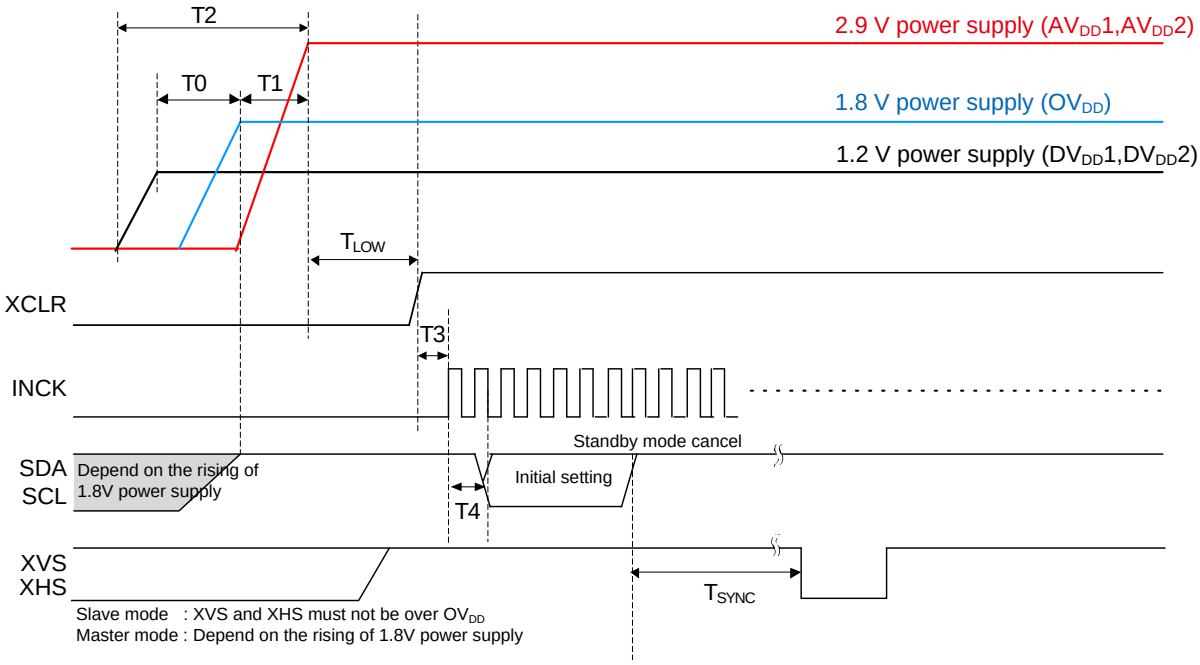
- ◆Change the number of vertical lines (In sensor master mode, change the VMAX. In sensor slave mode, change the period of XVS input.)
- ◆Horizontal and vertical scan direction. (When the vertical scan direction is changed, an invalid frame generates during transition.)
- ◆Change the mode between All-pixel scan and Window cropping. (However, It is case that transitions by not changing register HMAX . In addition, an invalid frame generates during transition.)

The changing MIPI lane setting can not support during sensor drive operation.

Power-on and Power-off Sequence

Power-on sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD1}, DV_{DD2}) →1.8 V power supply (OV_{DD}) → 2.9 V power supply (AV_{DD1}, AV_{DD2}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
3. The system clear is applied by setting XCLR to High level. The maser clock input after setting the XCLR pin to High level.
4. Make the sensor setting by register communication after the system clear.

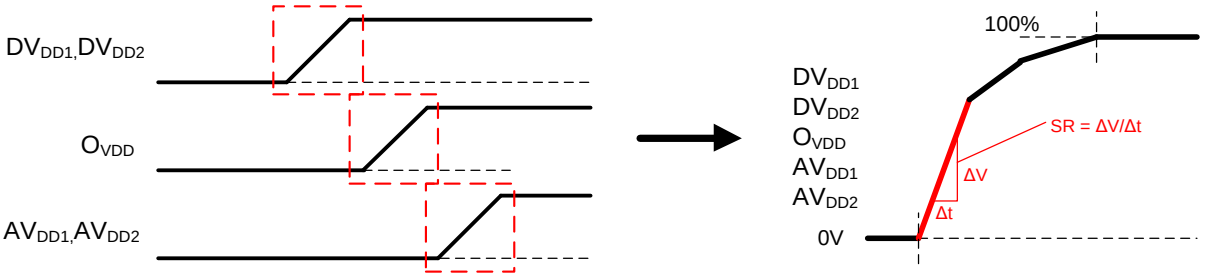


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 2.9 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
2.9 V power supply rising → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → INCK rising	T3	0	—	µs
Clear OFF → Communication start	T4	20	—	µs
Standby OFF (communication) → External input XHS,XVS (slave mode only)	T_{SYNC}	18	—	ms

Slew Rate Limitation of Power-on Sequence

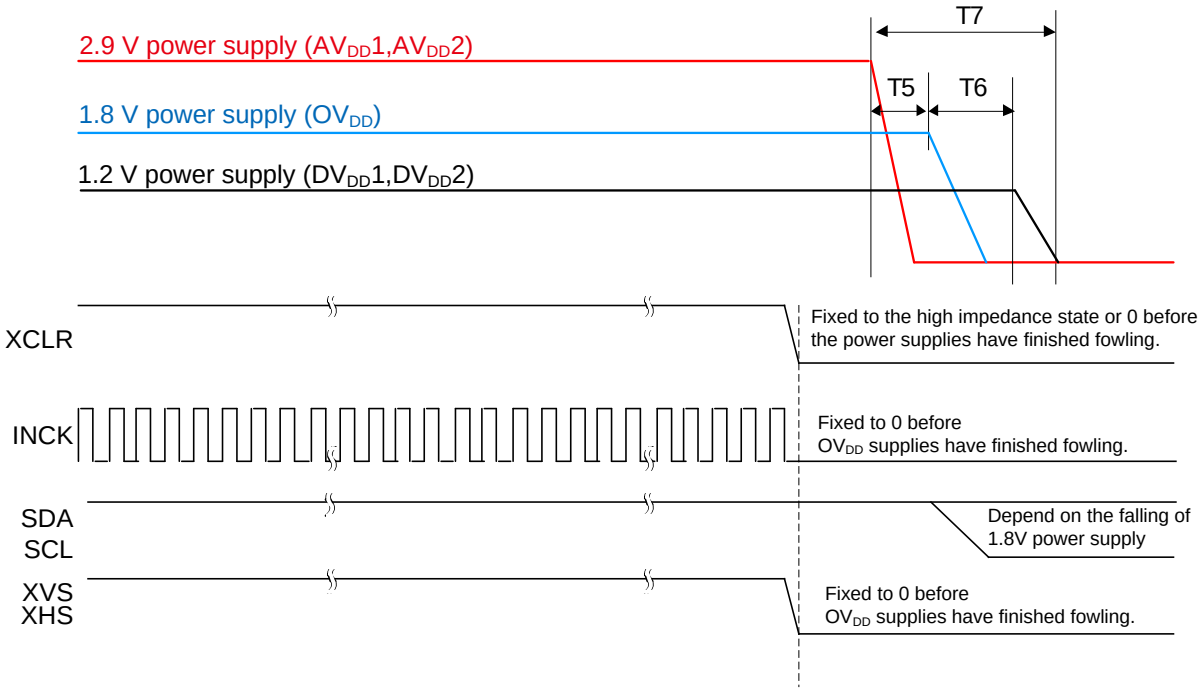
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD1} ,DV_{DD2}(1.2 V)	—	25	mV/μs	
		OV_{DD} (1.8 V)	—	25	mV/μs	
		AV_{DD1} ,AV_{DD2}(2.9 V)	—	25	mV/μs	

Power-off sequence

Turn Off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD1}, AV_{DD2}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD1}, DV_{DD2}). In addition, all power supplies should falling within 200 ms. Set each digital input pin (INCK, SDA, SCL, XCLR, XMASTER, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



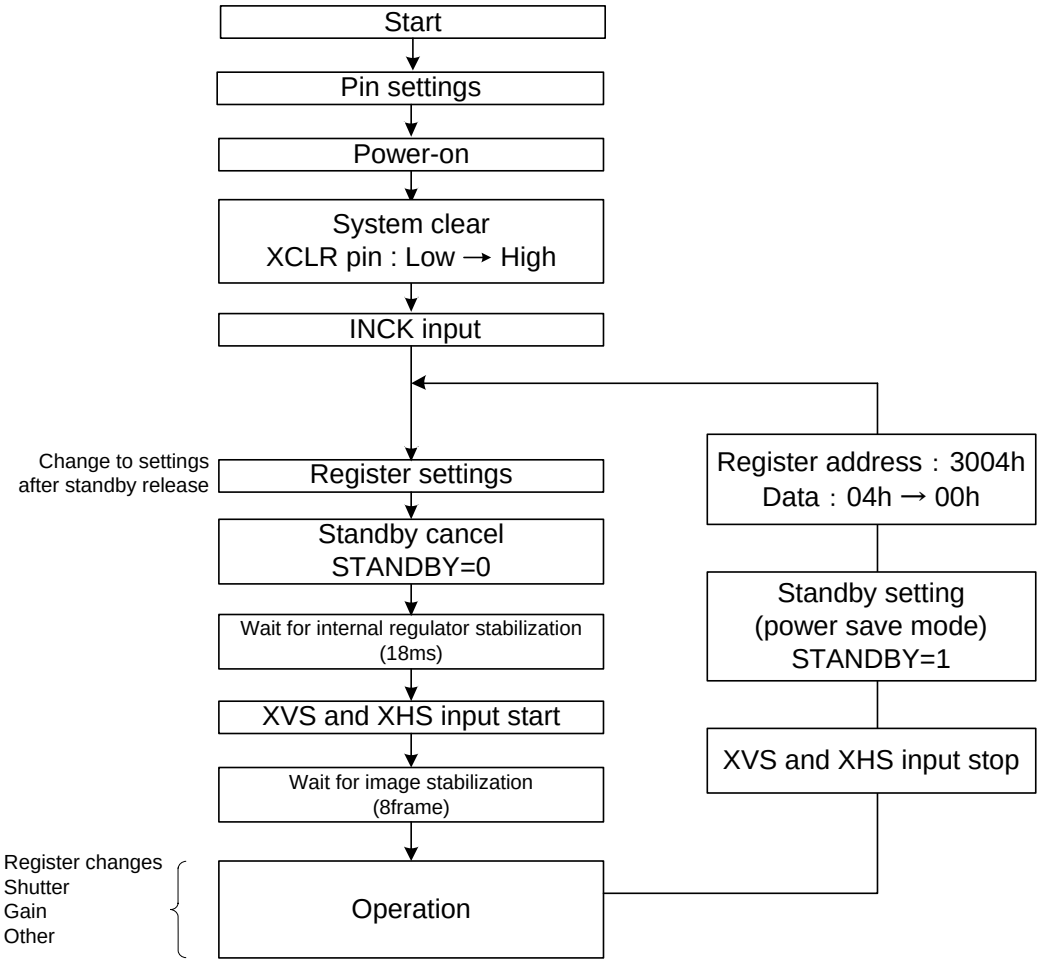
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
2.9 V power shut down → 1.8 V power shut down	T5	0	—	ns
1.8 V power shut down → 1.2 V power shut down	T6	0	—	ns
Shut down time of all power supply	T7	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

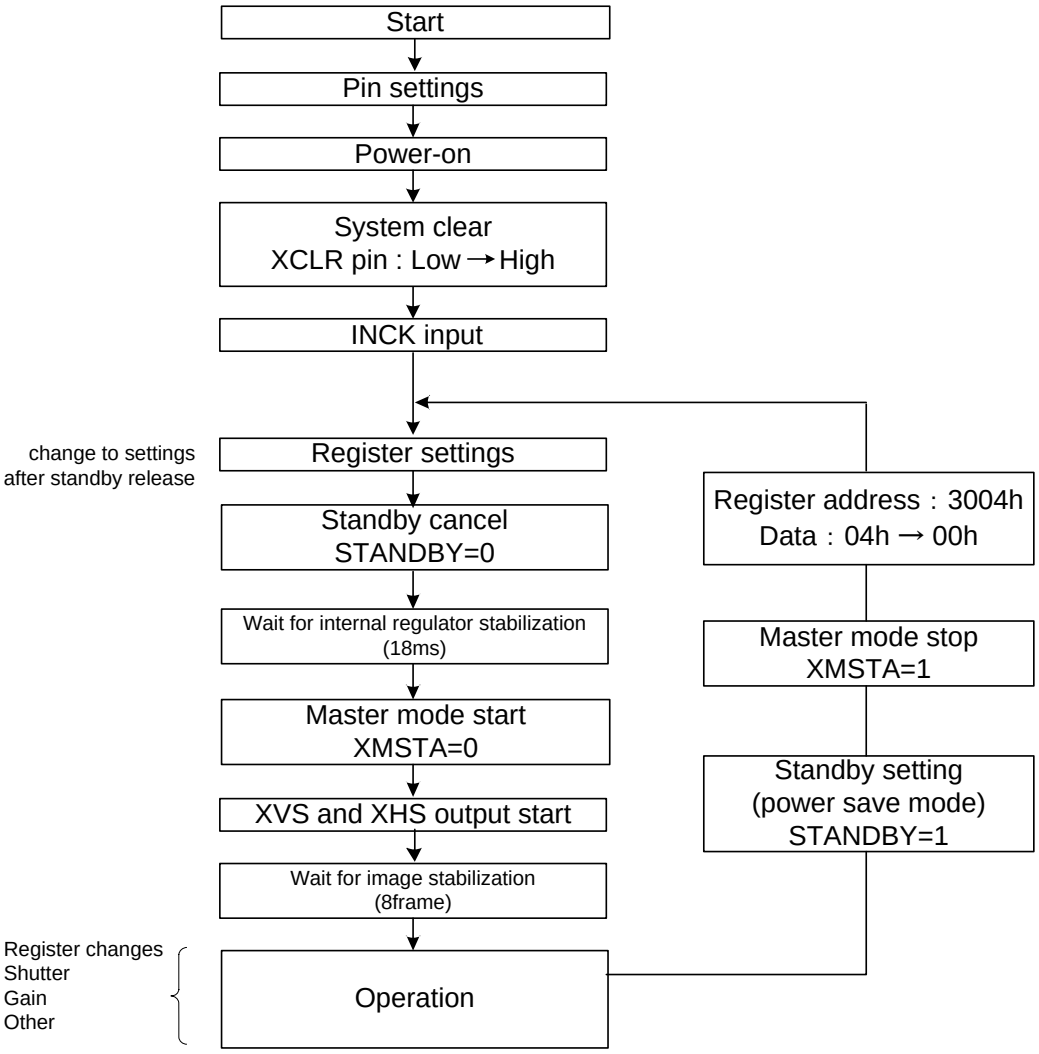
The figure below shows operating flow in sensor slave mode.
For details of "Power-on" to "Reset cancel", see the item of "Power-on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

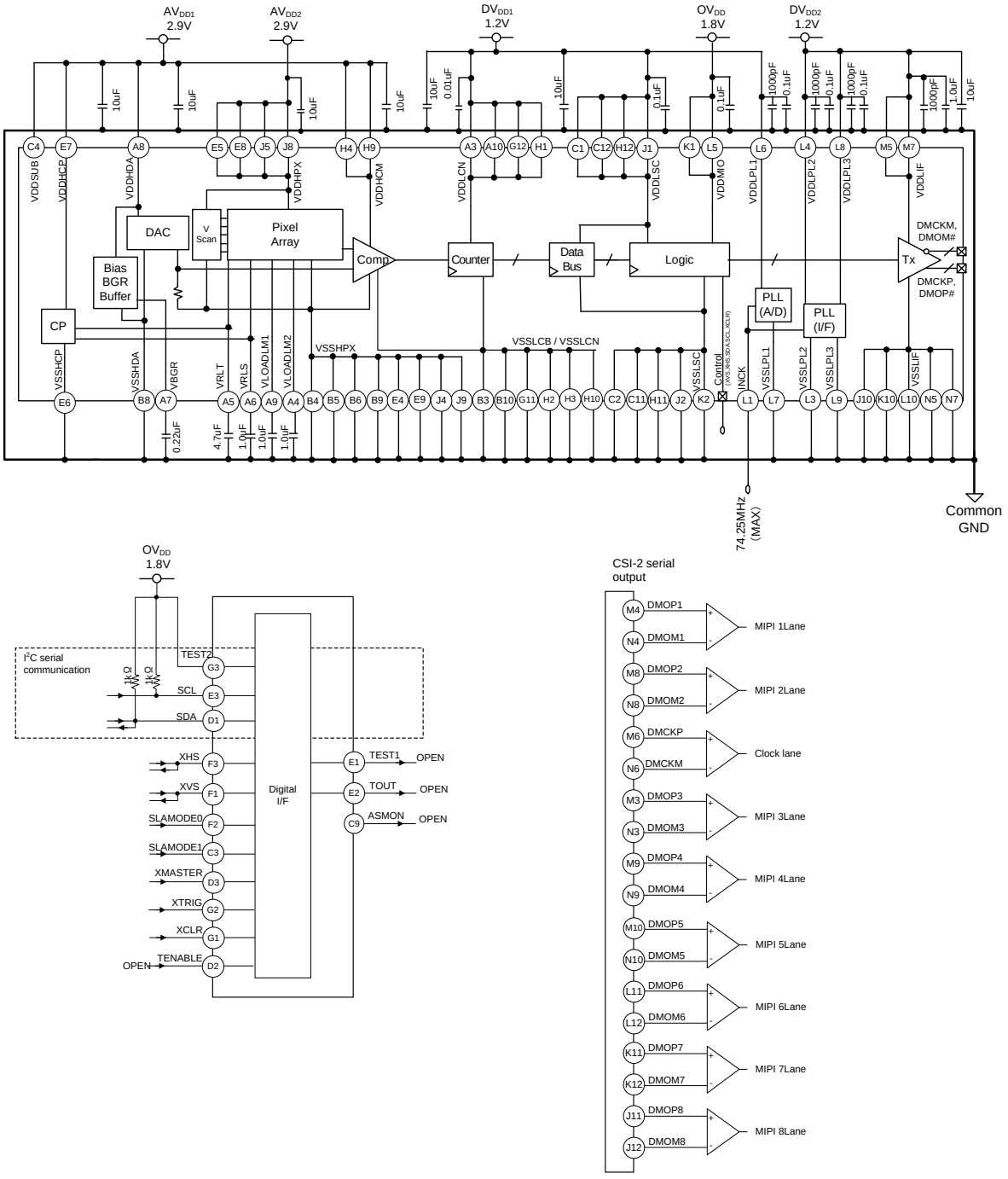
Setting Flow in Sensor Master Mode

The figure below shows operating flow in sensor master mode.
For details of "Power-on" to "Reset cancel", see the item of "Power on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
In master mode, “Master mode start” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

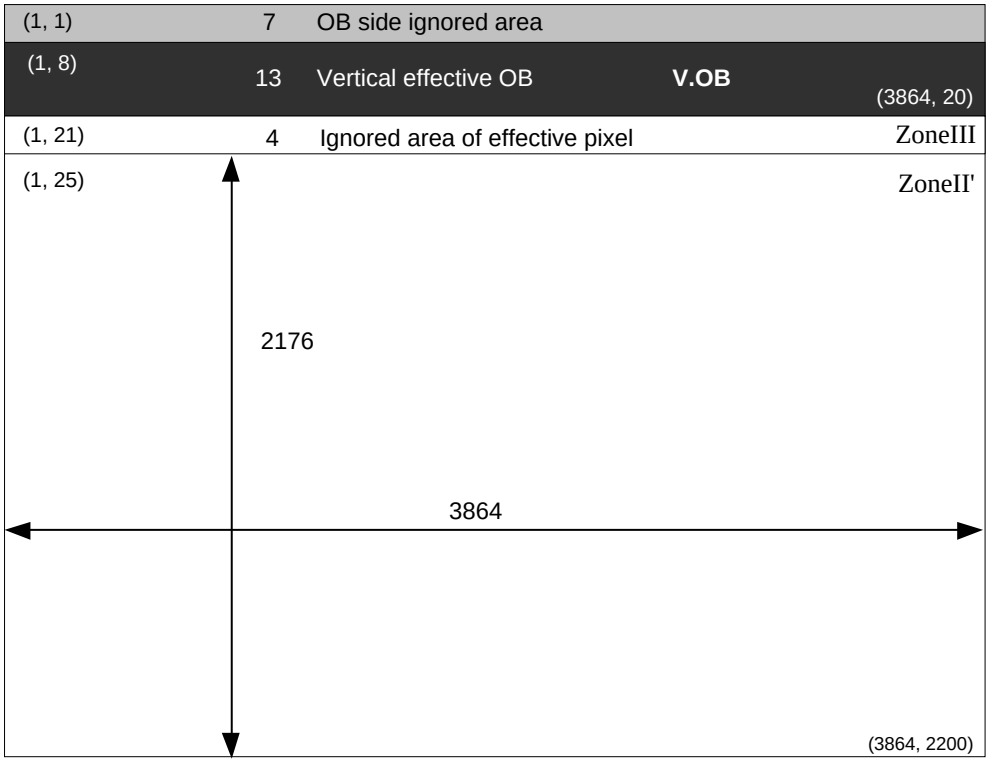
Spot Pixel Specifications

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30% ≤ D	60	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	800		No evaluation criteria applied		2	1/30 s storage
Black pixels at signal saturated	D ≤ 715 mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, particle radiation such as cosmic rays etc. may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".)
Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C)	Annual number of occurrence
5.6 mV or higher	30 pcs
10.0 mV or higher	17 pcs
24.0 mV or higher	7 pcs
50.0 mV or higher	3 pcs
72.0 mV or higher	2 pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

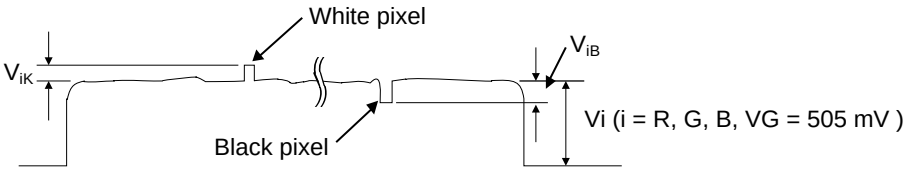
Material_No.03-0.0.10

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adKusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 505 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

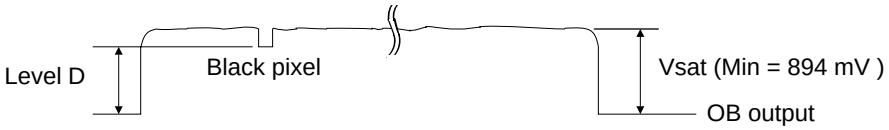
   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

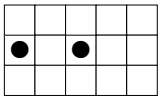
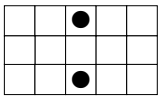


Signal output waveform of R/G/B channel

Spot Pixel Pattern Specification

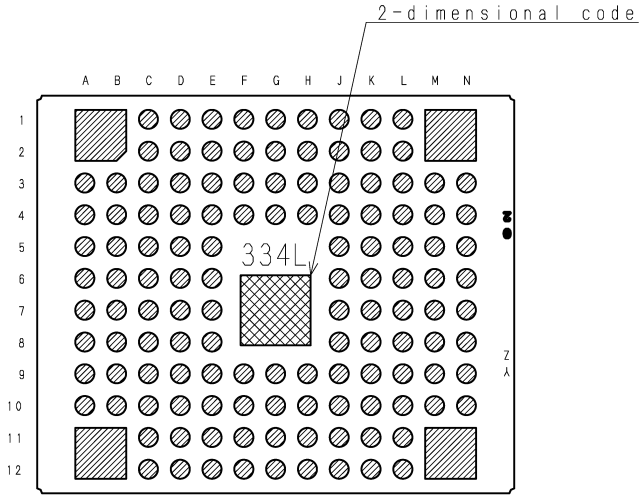
White Pixel, Black Pixel and Bright Pixel are Kudged from the pattern whether they are allowed or reKected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern  It provides by color filter array described in the left.	White pixel Black pixel Bright pixel
1	 Same color	Rejected
2	 Same color	Rejected

Note) 1.”●” shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not Kudged to be reKected.)
2. When one or more spot pixels indicated “ReKected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking



Note:Following characters enter into "Y", and"Z". (No Au coat)
Y:In English upper case character, One character
Z:Number, single number

DRAWING No. AM-B334LQR(2D)

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

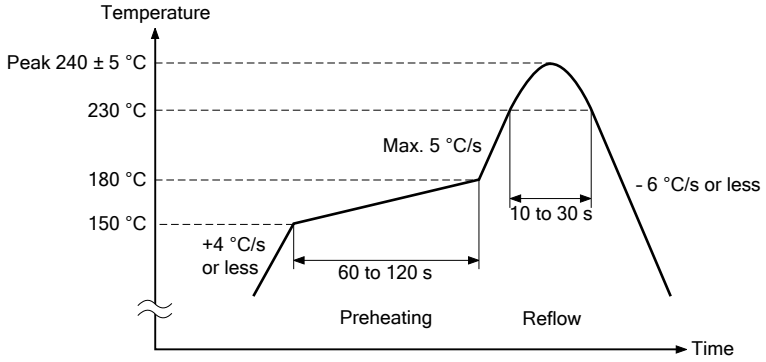
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (- 6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

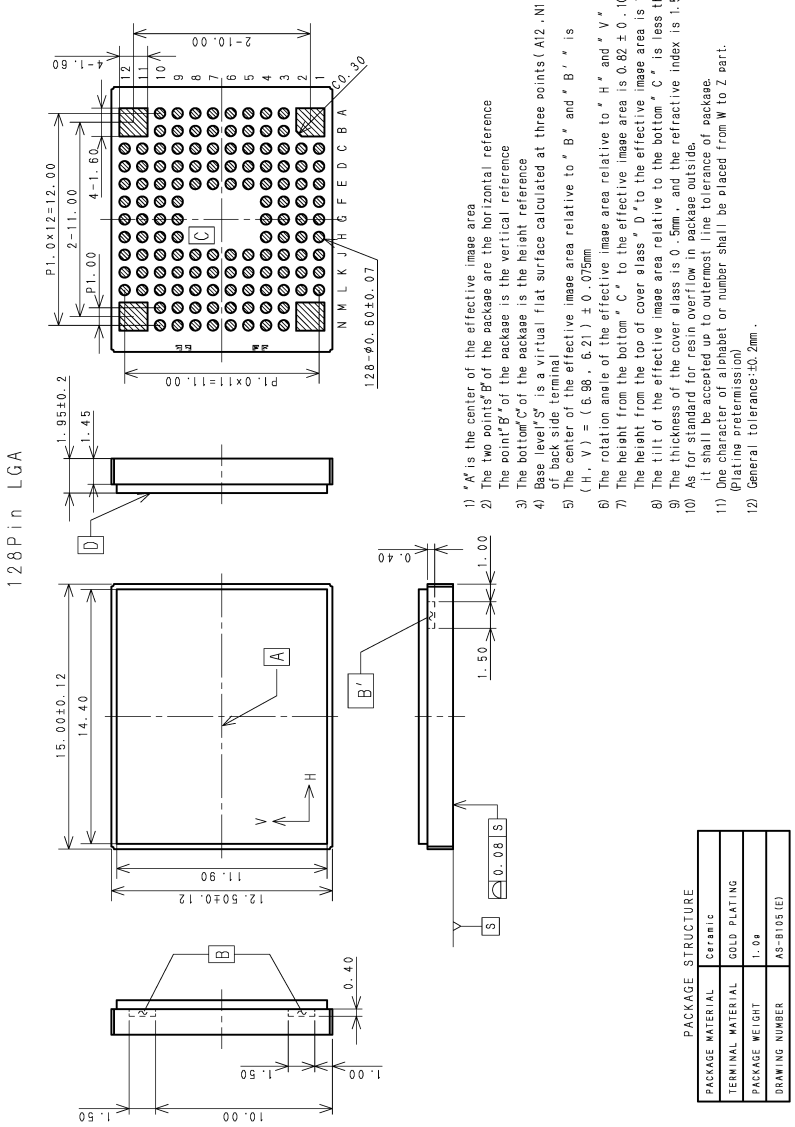
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Material_No.14-0.0.6

Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

STARVIS

* STARVIS is a trademark of Sony Corporation. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for surveillance camera applications. It features a sensitivity of 2000 mV or more per 1 μm^2 (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

Revision History

Date of change	Ver	Page	Contain of Change
2017/05/19	0.1	–	First Edition
2017/10/30	0.2	1	Update ; Gain setting range in CDS / PGA function WDR → HDR name changed.
		11	Correction ; Pin description Pin No C9 I/O : Power → O Description : Reference pin → TEST output pin
		16	Update ; Current consumption
		19	Correction ; I^2C Specification VOL, VOH Low level input voltage → Low level output voltage High level input voltage → High level output voltage
		20	Correction ; I/O Equivalent Circuit Diagram TOUT symbol deleted
		21	Update ; Spectral sensitivity characteristics
		22	Update ; Image sensor characteristics
		24	Correction ; Sensitivity ratio, saturation signal and Video signal shading Gr and Gb signal outputs 650mV → 505mV
		25	Correction ; SLAVE address list SLAMODE1 → SLAMODE0
		31	Correction ; the immediate reflection registers XMSTA added
		40	Update ; Register address 30E8h, 30E9h setting range TBD → 72.0dB
		42	Correction ; Register address 3199h Horizontal/Vertical 2/2-line binning 1 → 3
		43	Correction ; SYS_MODE setting 1h : 1728Mbps → 1h : 1188Mbps 3h : 891Mbps → 2h : 891Mbps Register address 31A1h XVS_DRV, XHS_DRV added
		45 to 53	Update ; Added the register which shoud be chaged the value from the default value after the reset
		58,61	Correction ; VALID_EXPAND register address 31DCh → 31DDh
		64	Correction ; Y_OUT_SIZE register added in window cropping mode
		68	Update ; Normal image output TBD → 8frames Correction ; Sequence from Standby Cancel to Stable Image Output figure Signal XCE → SCL
		69	Correction ; XVS_DRV and XHS_DRV added in list of register master mode
		71	Update ; Gain setting range TBD → 72.0dB
		83	Correction ; INCK 27MHz setting added

Date of change	Ver	Page	Contain of Change
2017/10/30	0.2	84	Correction ; Register Hold Setting figure Register setting timing 12H → 6H FS output timing 12H → 10H
		85	Correction ; Power-on sequence No3 XCE control description deleted. T_{SYNC} 20ms → 18ms
		88,89	Update ; Wait time added
		90	Correction ; Control signal XCE deleted. SDI, SCK → SDA,SCL VDDD2 1.8V → OVDD1.8V
		91	Update ; Spot pixel specifications
		93	Correction ; Black or white pixels at high light Gr and Gb signal outputs 650mV → 505mV Black pixels at signal saturated Vsat Min =913mV → 894mV
		97	Update ; Recommended reflow soldering conditions
2017/12/04	E17Y08	32	Added ; Register 3004h
		51	Update ; Register address 37B0h XMASTER pin low setting added.
		58	Correction ; 4lane 1782Mbps / lane frame rate 30/25 frame/s → 60/50 frame/s
		62	Correction ; Vertical inverted register setting 30A4h, 30A5h 03h → 33h
		64,65	Added ; Inverted register setting in window cropping mode
		92	Update ; The annual number of white pixels occurrence updated.
		95	Update ; Marking figure
		98	Update ; Package outline
2018/04/11	E17Y08A84	2	Correction ; Device structure total number of effective pixels 8.41Mpixels → 8.42Mpixels
		15	Correction ; VOH, VOL electrical characteristics VOH min : OV_{DD} – 0.4 → OV_{DD} – 0.2 VOL max : 0.4 → 0.2
		18	Correction ; XVS – XHS fall width 1 / f_{INCK} → 0ns Added ; XVS / XHS Tr and Tf
		32,33,42,43	Correction ; 300Ch, 300Dh, 315Ah, 3168h, 316Ah, 319Eh register description
		56	Added ; Embedded data bit assign

Date of change	Ver	Page	Contain of Change
2018/04/11	E17Y08A84	58	Correction ; All-pixel scan mode 4lane 1782Mbps/lane HMAX setting 044Ch / 0528h → 0226h / 0294h
		65	Added ; AREA3_ST_ADR_1 register setting way Correction ; V_{TTL} calculation formula AREA3_WIDTH_1 ×2 + 48 → AREA3_WIDTH_1 + 48 1H period on Window cropping mode “Number of INCK in 1H” → “1H period”
		66	Correction ; Example of Window cropping Mode Setting
		68	Correction ; Stable image output timing 8frame → 9frame